Laboratory of Superconducting Devices for Signal Detection and Processing

Kotel'nikov Institute of Radio Engineering and Electronics, Moscow, Russia

Valery Koshelets

Superconducting technology for integrated receivers; frontend and backend components

Questions to be answered:

- Can superconducting integrated receiver (SIR) play a role in future heterodyne arrays?
- Can superconducting digital components play a role as fast digitizers and/or in a backend spectrometer?

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Pavel Dmitriev, Andrey Ermakov, Lyudmila Filippenko, Mikhail Fominsky, Konstantin Kalashnikov, Nickolay Kinev, Oleg Kiselev, Kirill Rudakov, Sergey Shitov, Alexander Sobolev, Mikhail Torgashin

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NOVA, University of Groningen, the Netherlands

SRON Netherlands Institute for Space Research

university of groningen

Andrey Baryshev, Dick Boersma, Johannes Dercksen, Hans Golstein, Thijs de Graauw, Leo de Jong, Andrey Khudchenko, Jacob Kooi, Arno de Lange, Gert de Lange, Willem Lauinge, Pavel Yagoubov

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Yokohama University, Japan

NY State University at Stony Brook, NY, USA

Moscow State University, Moscow, Russia

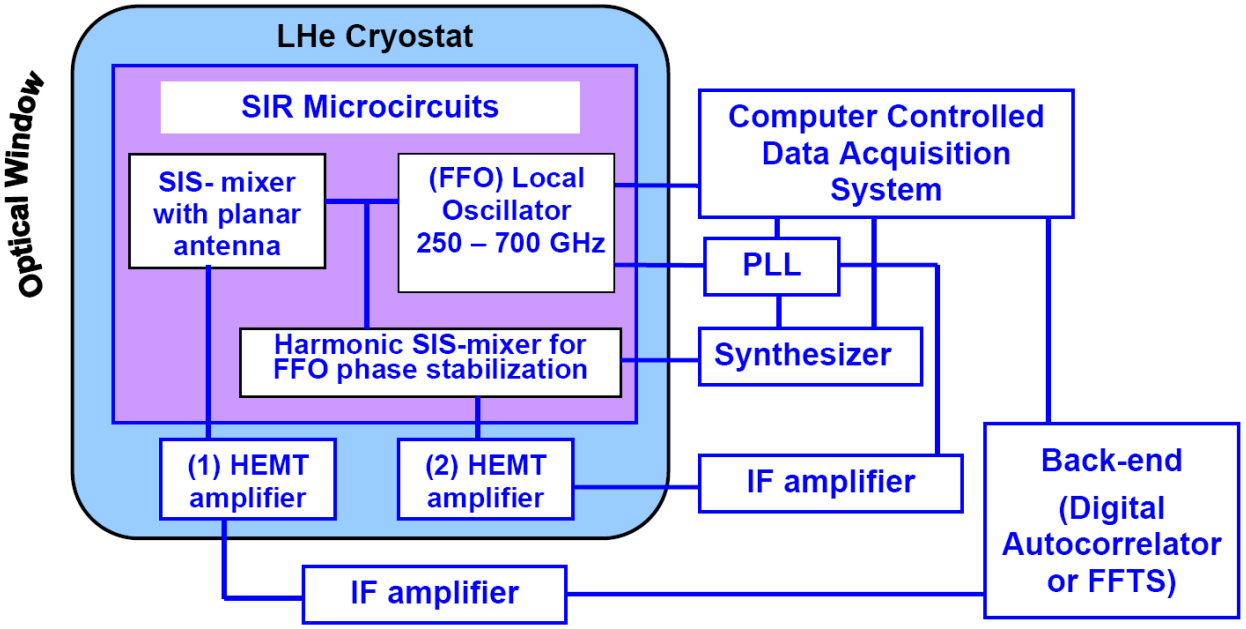
Timur Filippov, Nobuyuki Yoshikawa, Vasili Semenov, Igor Solov'ev

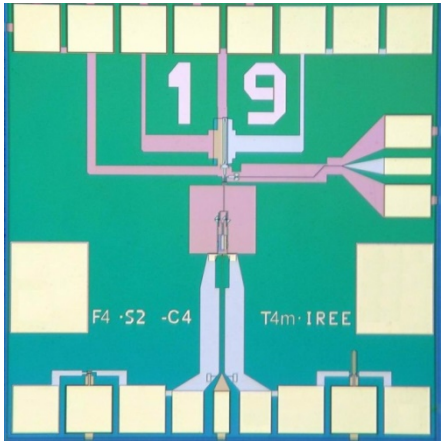
Superconducting technology for integrated receivers; frontend and backend components

Outline

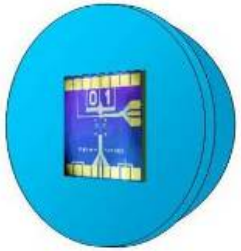
- **Superconducting Integrated Receiver (SIR); TErahertz LImb Sounder (TELIS) project; Lab applications**
- **Flux-Flow Oscillator as on-chip superconducting LO: advantages and problems**
- **Superconducting digital components for backend spectrometer**

Superconducting Integrated Receiver (SIR) with phase-locked FFO

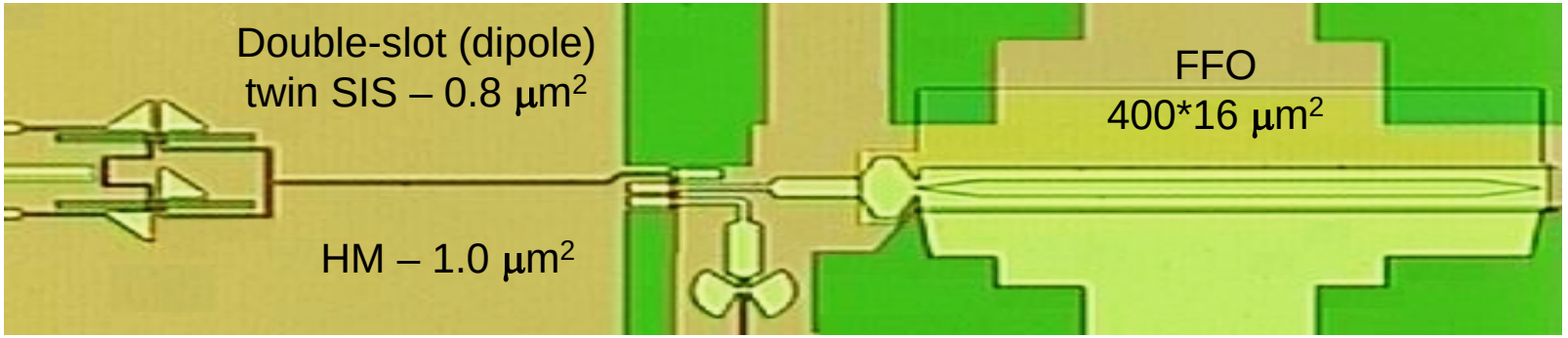




SIR microcircuit



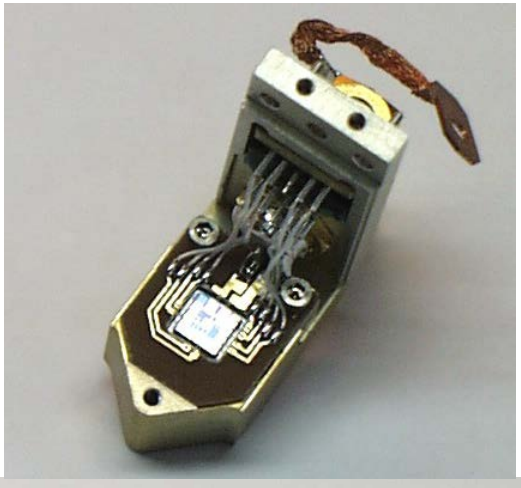
Nb-AlOx-Nb, Nb-AlN-NbN; Jc = 5 - 10 kA/cm²



Superconducting Integrated Receiver (SIR)

STATE OF THE ART (2002)

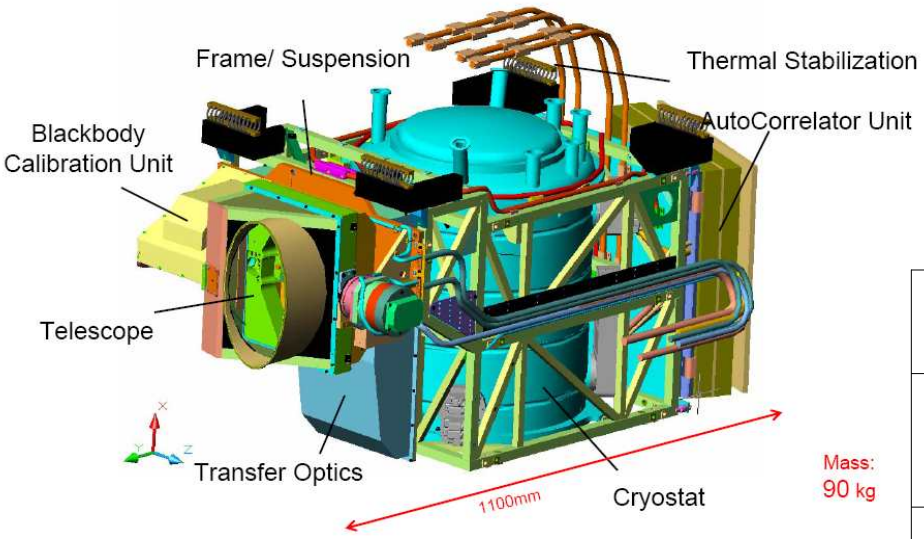
- Single chip Nb-AlOx-Nb SIS receivers with superconducting FFO have been studied at frequencies from 100 to 700 GHz;
- A DSB receiver noise temperature as low as 90 K has been achieved at 500 GHz;
- 9-pixel Imaging Array Receiver has been successfully tested;
- FFO Phase Locking (PLL) up to 700 GHz.

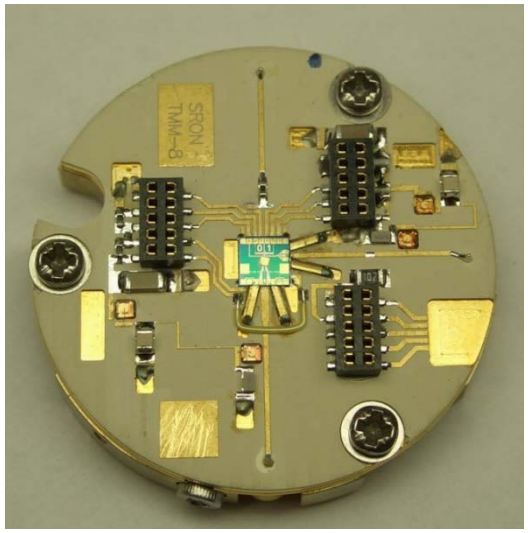


APPLICATIONS

- Airborne Receiver for Atmospheric Research and Environmental Monitoring; Radio Astronomy
- Focal Plane Array Receivers;
- Laboratory submm wave Spectrometers.

TELIS (Terahertz Limb Sounder)





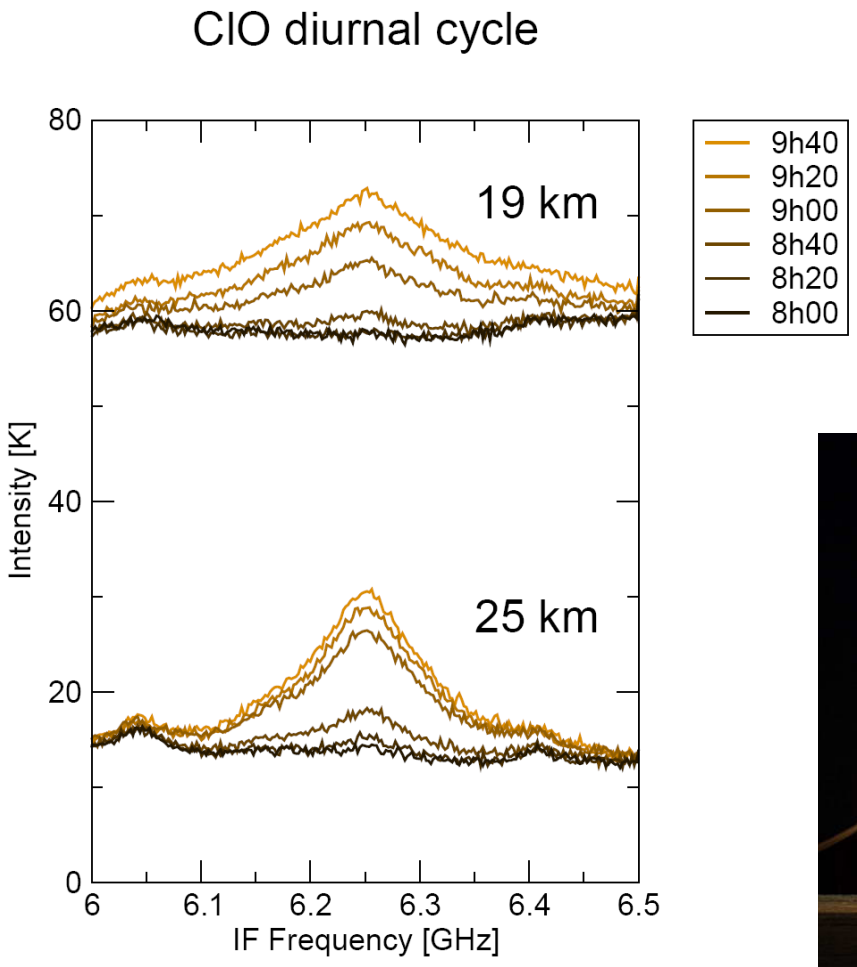
Balloon-Borne TELIS Instrument

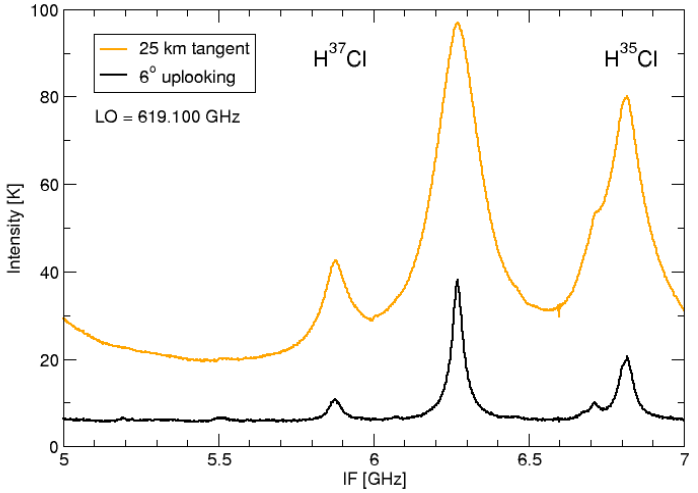
TELIS-SIR Main Parameters

Input frequency range	470 – 670 GHz
Minimum DSB noise temperature	< 120 K
Output IF range	4 - 8 GHz
Spectral resolution	< 1 MHz
System stability (Allan variance)	20 s
Dissipated power (at 4.2 K stage)	< 30 mW
Operation temperature	< 4.5 K

4 TELIS flights; Esrange, Sweden; Canada

(ClO level = 2.1 ± 0.3 ppbv; BrO – 0.3 K = a few pptv)

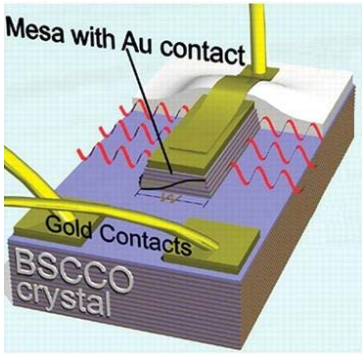


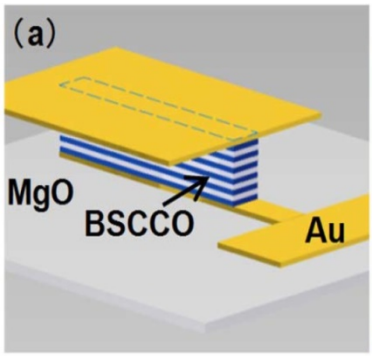


THz emission from a BSCCO mesa measured by the SIR

In collaboration with Prof. Huabing Wang

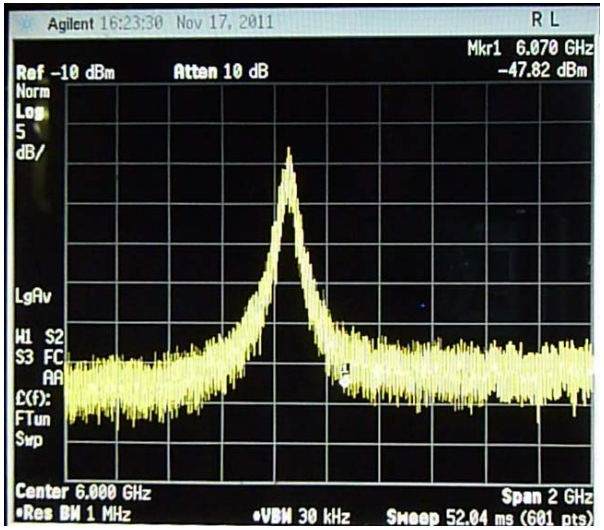
Research Institute of Superconductor Electronics, Nanjing University, China
National Institute for Materials Science, Tsukuba 3050047, Japan

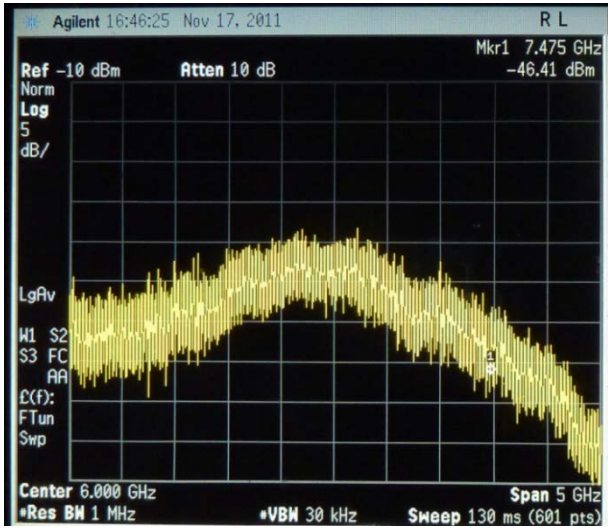




M. Ji, et al, Phys Rev B (2012);
D.Y. An, et al, Appl Phys Lett (2013);
B. Gross, et al, Phys Rev B (2013);
M. Ji, et al, Appl Phys Lett (2014);
L.J. Hao, et al, Phys Rev Applied (2015);
F. Rudau, et al, Phys Rev Applied (2016);
O. Kizilaslan, et al, SUST (2017)

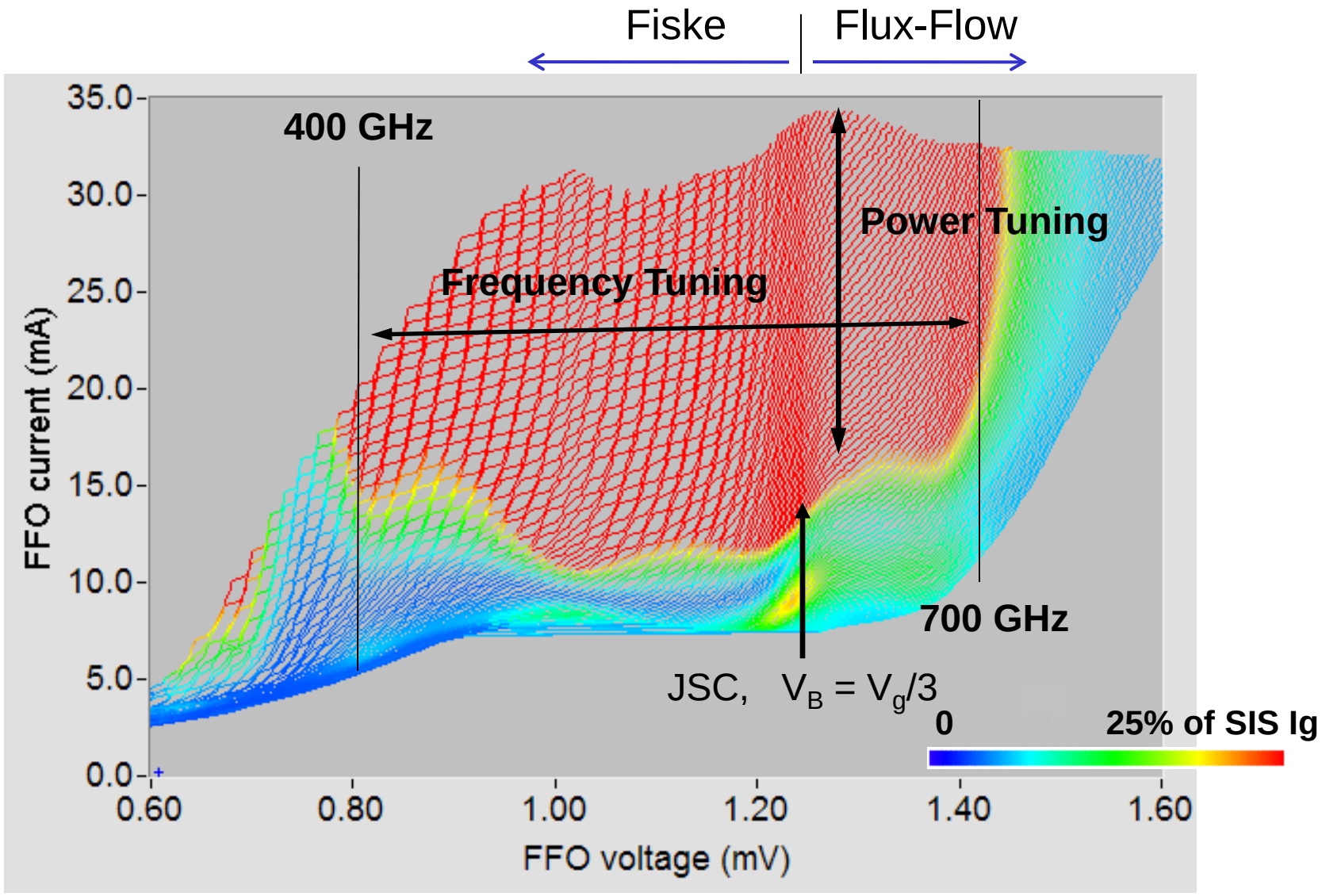
Frequency range : 420 ~ 735 GHz; Linewidth: down to 7 MHz; PLL



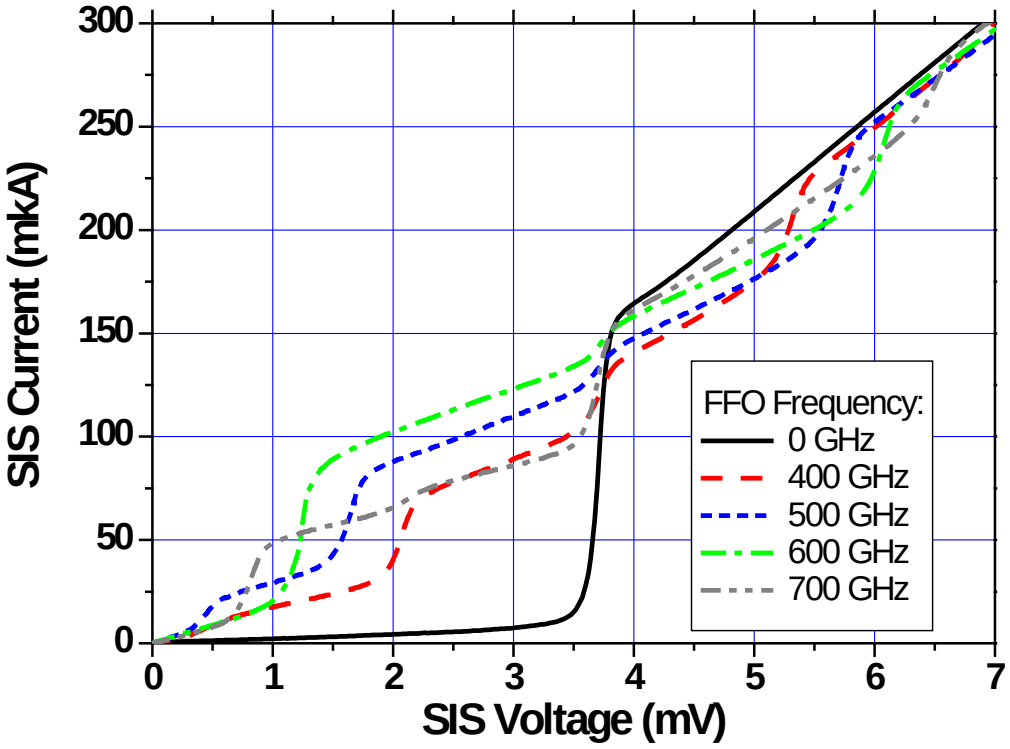


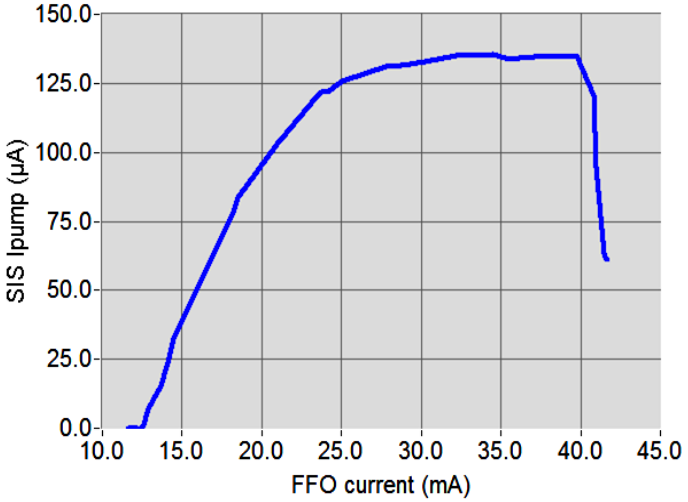
Emission above 1.7 THz; power as high as 610 μW at 500 GHz

Superconducting Flux Flow Oscillator (FFO)

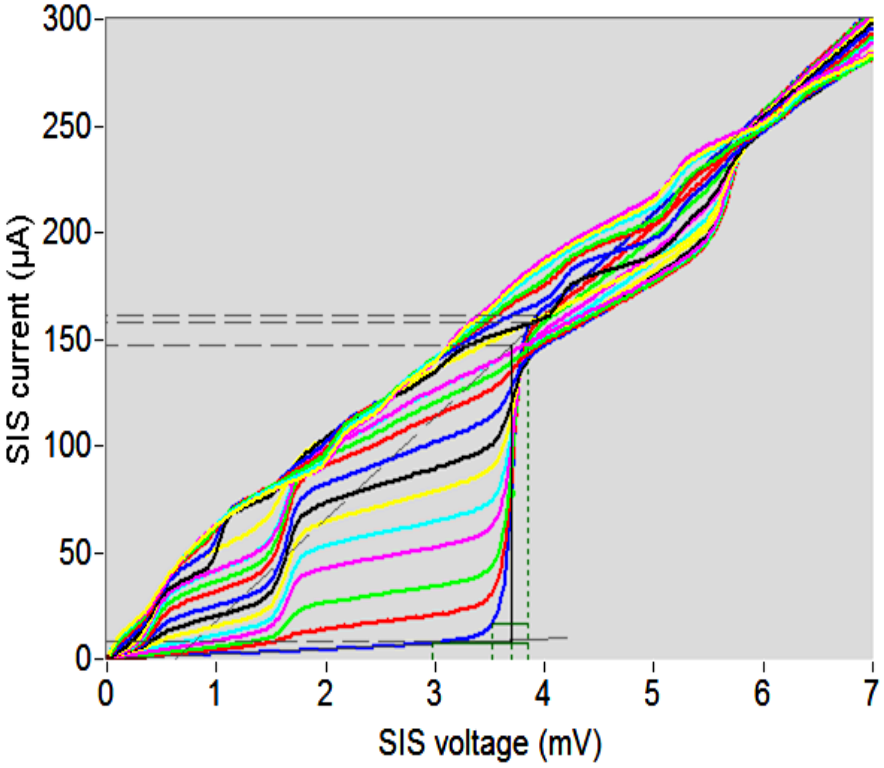


FFO frequency and power tuning

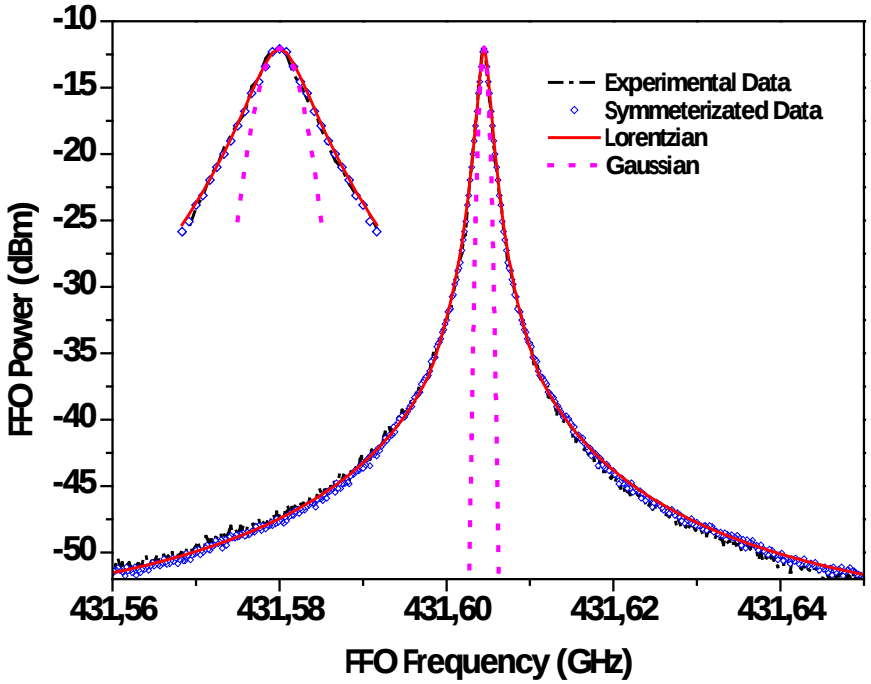


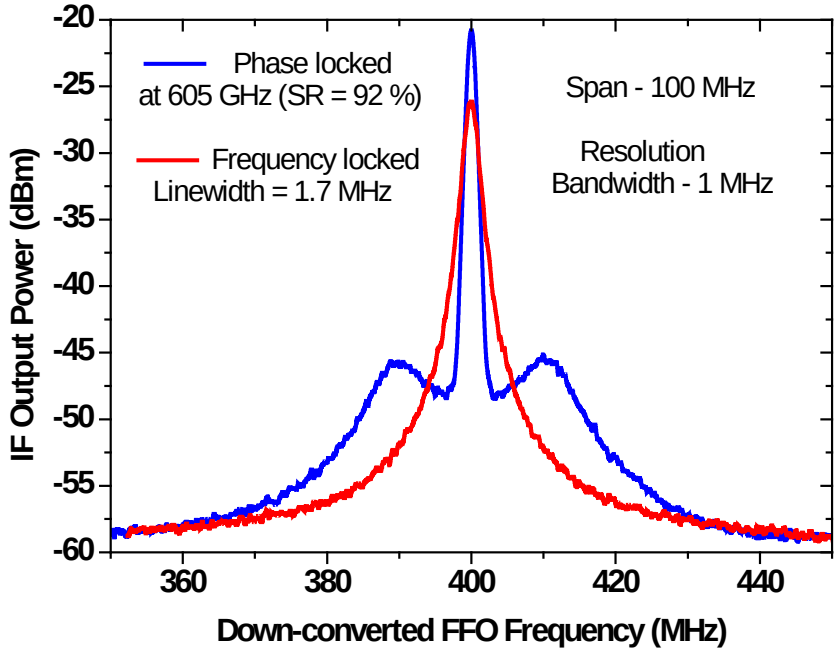


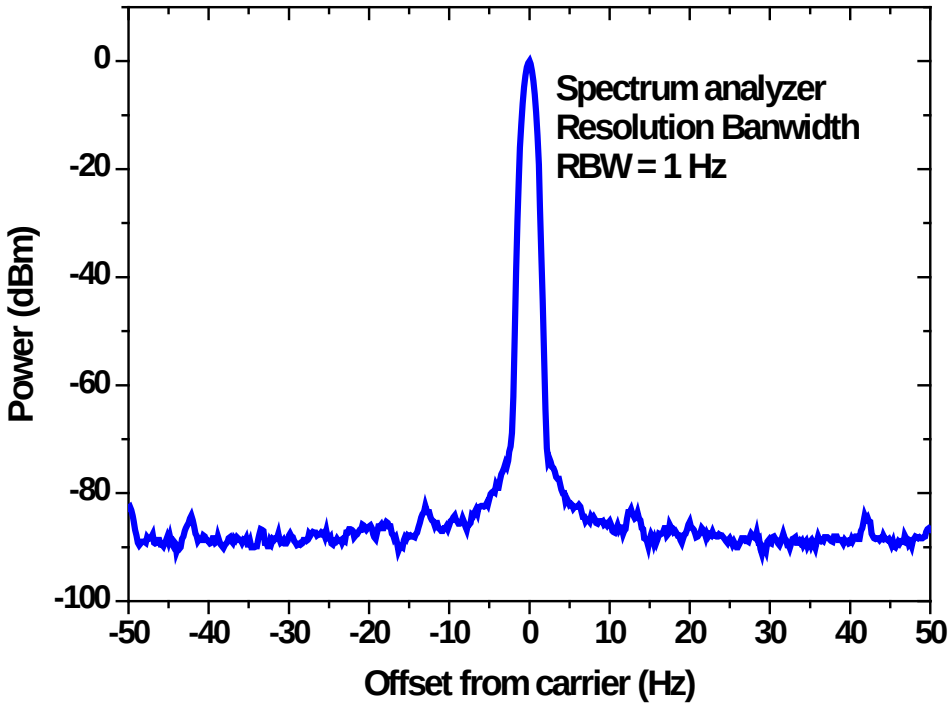
FFO frequency = 500 GHz



Spectra of the FFO





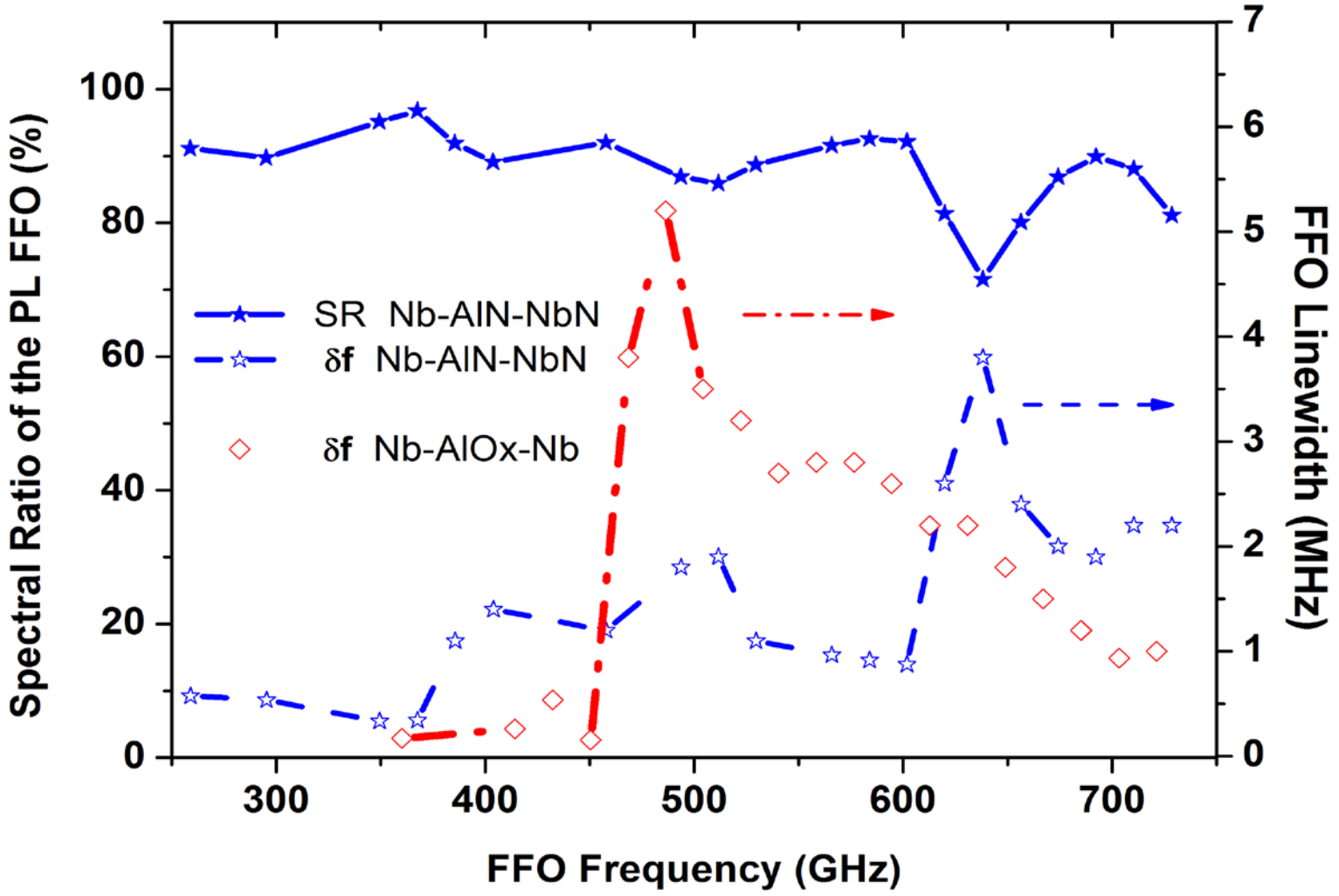


FFO frequency 605 GHz:

LW = 1.7 MHz; SR = 92 %;

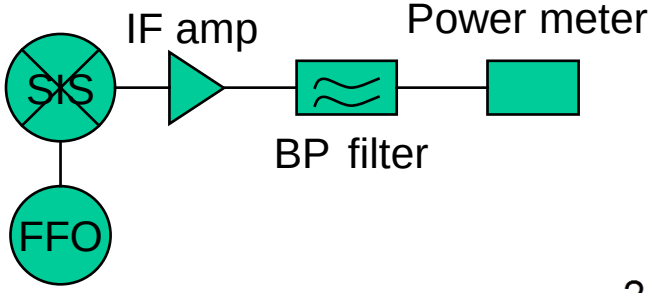
FFO phase noise -90 dBc/Hz

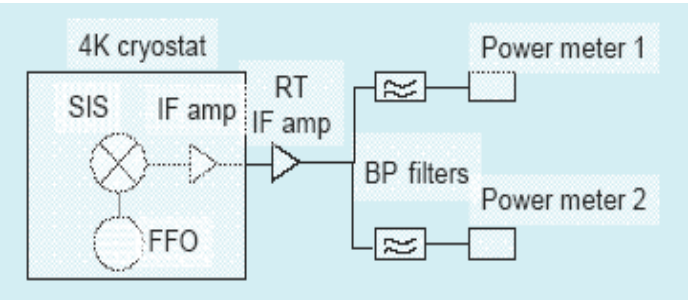
Linewidth and Spectral Ratio on the FFO frequency

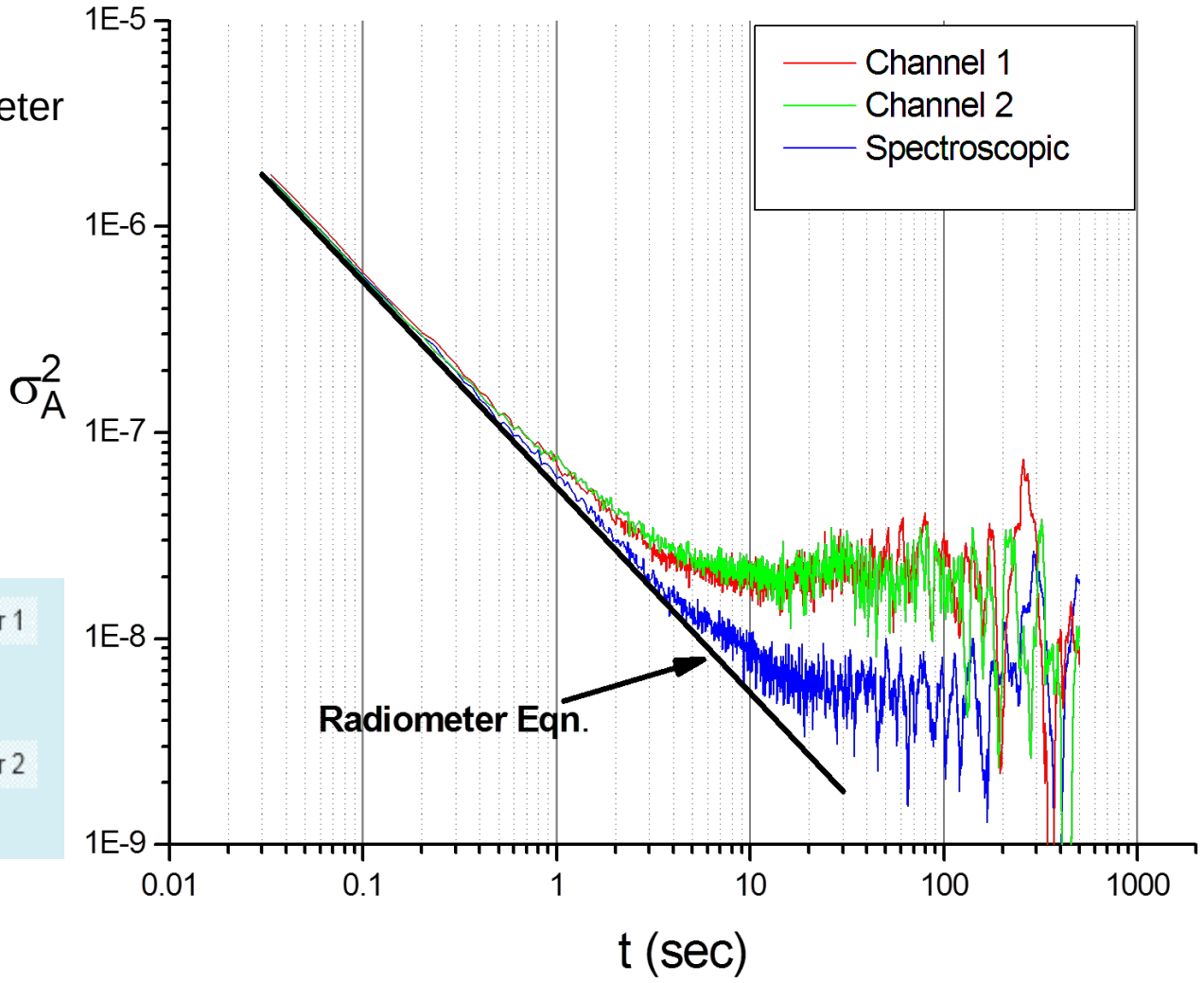


For ALMA interferometer the LO rms phase noise should be < 75 fs;
it requires the SR > 95 % at the frequency of about 600 GHz

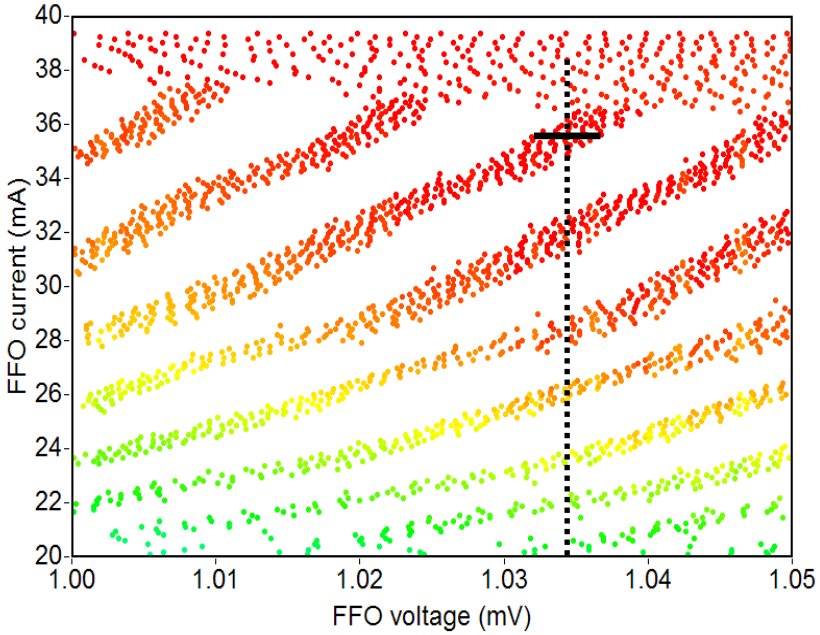
SIR Stability: Allan variance test

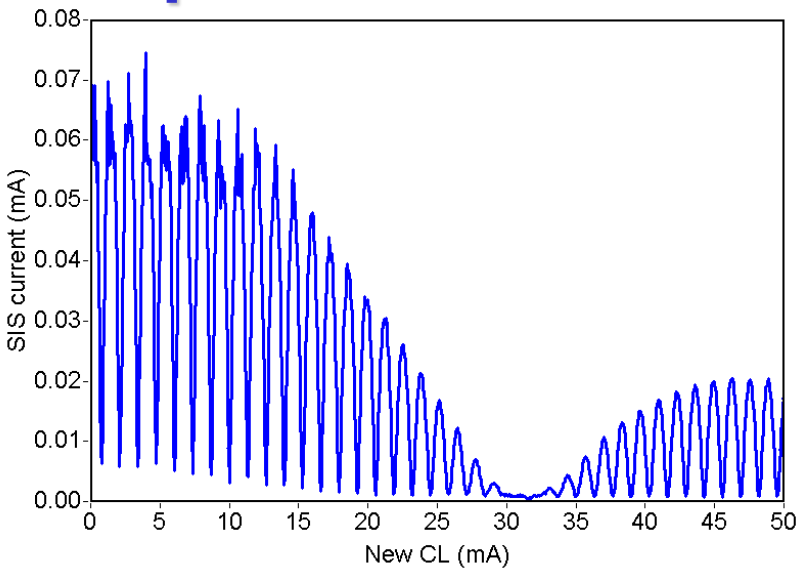


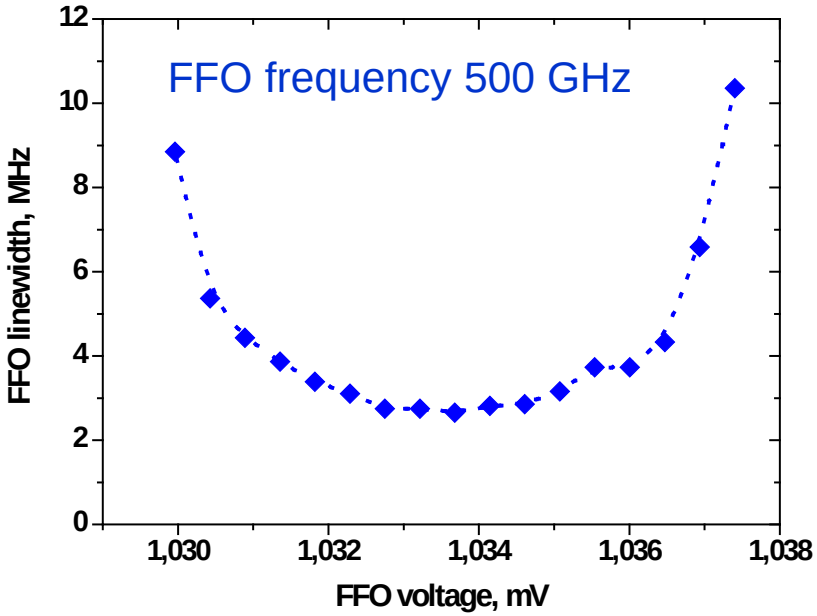


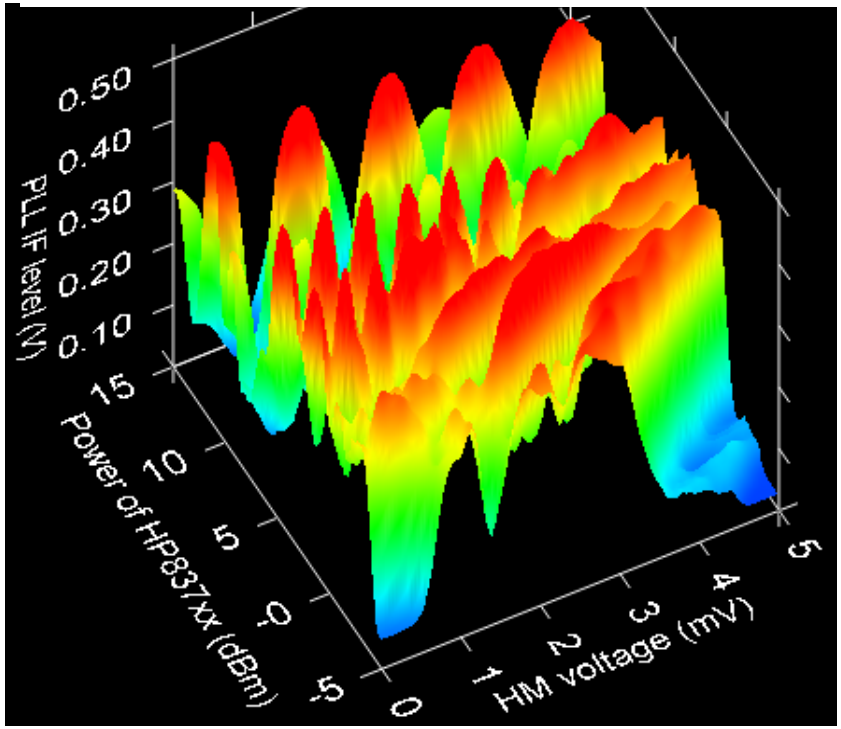


SIR for TELIS – remote operation



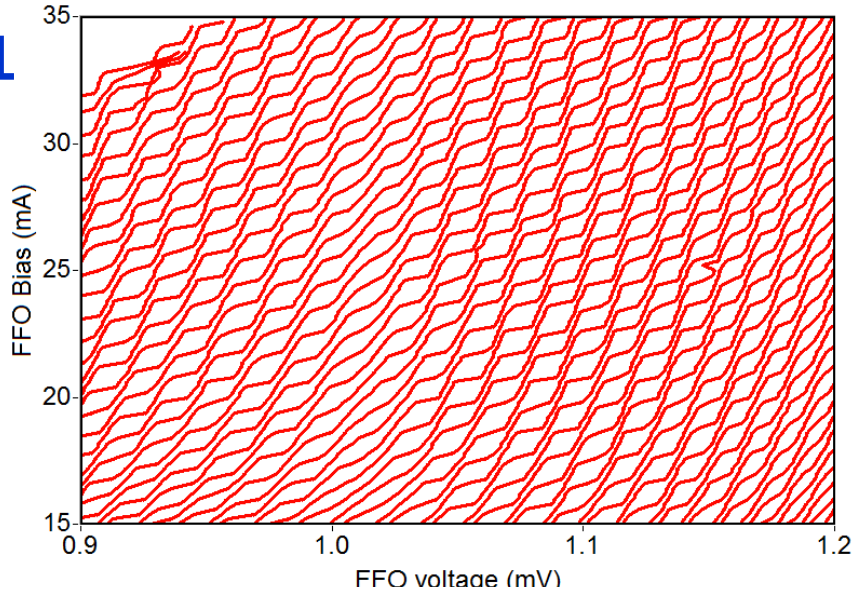


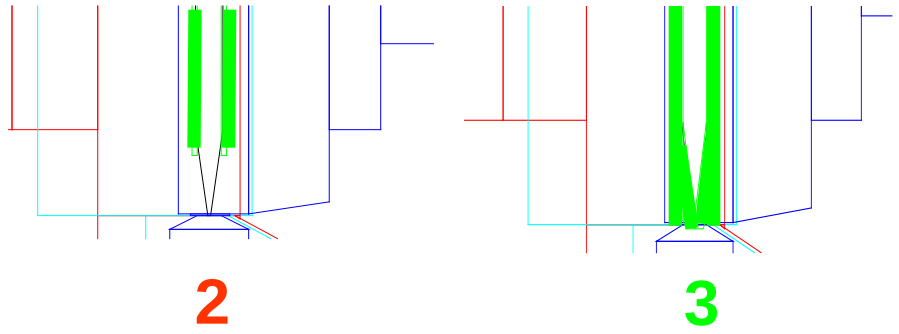




Suppression of the Fiske Steps

1

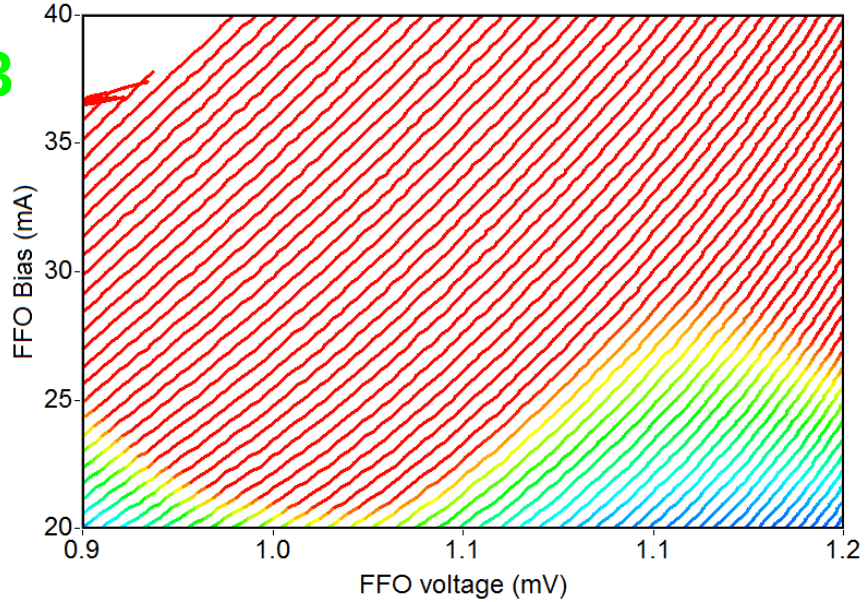


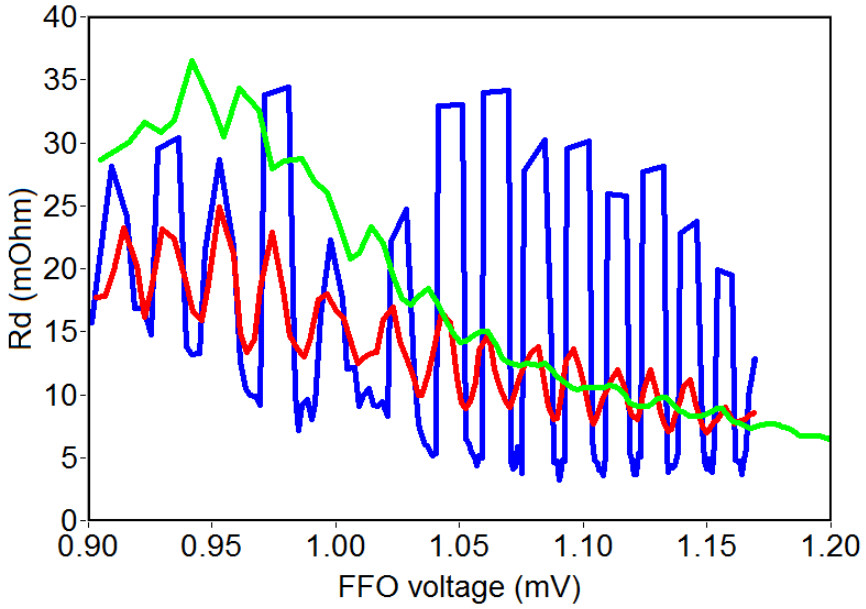


2 3

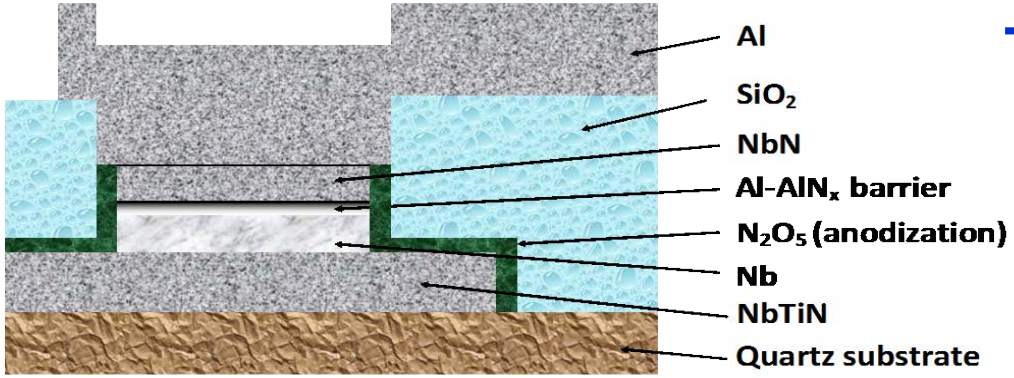
1 2 3

3



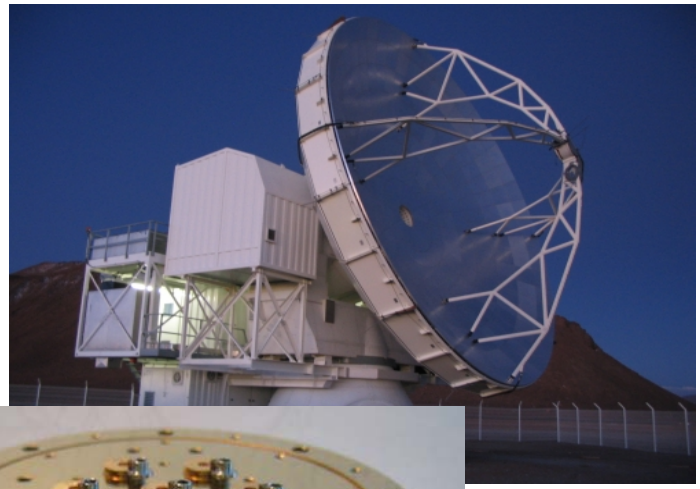


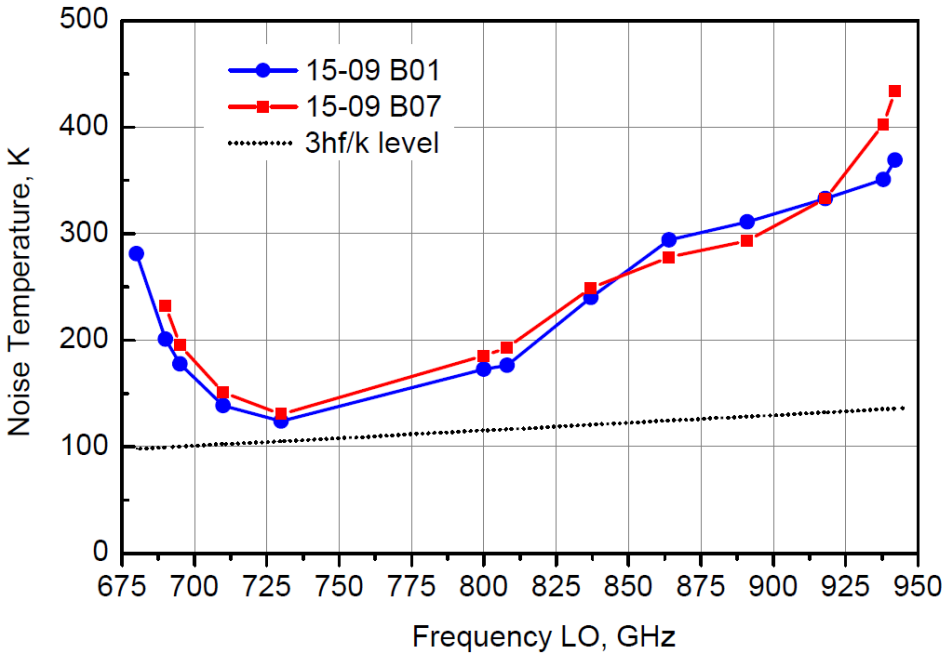
Extension of the SIR frequency up to 1 THz



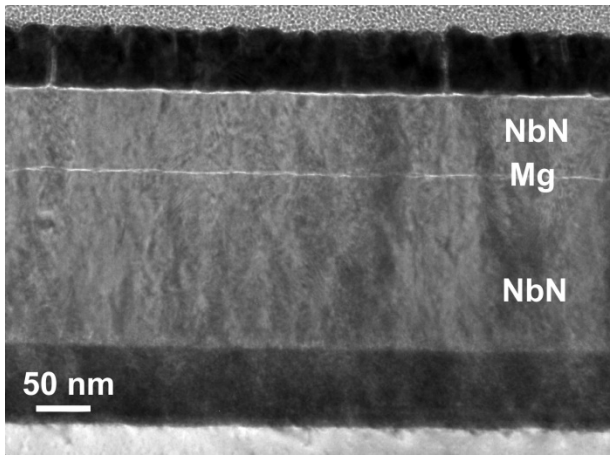
THz SIS Receiver for APEX

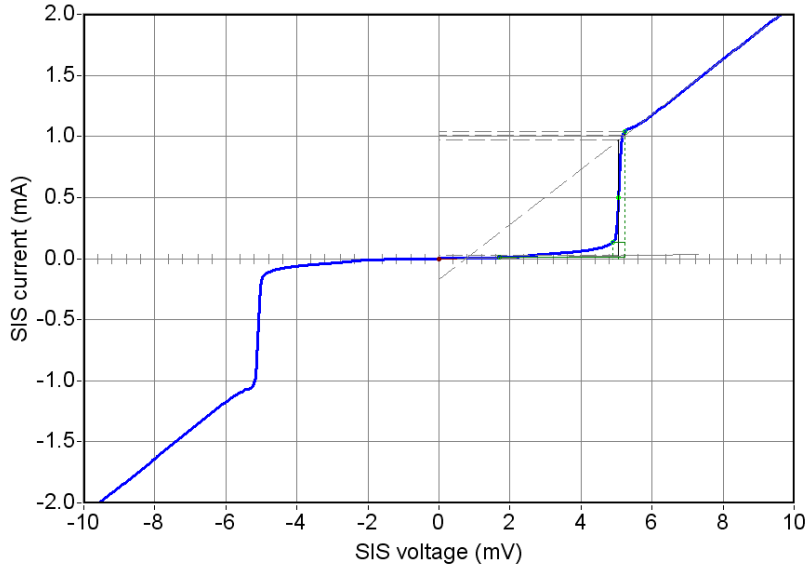
Nb/Al-AlN_x/NbN SIS
(A = 0.5 μm²; Jc ~ 30 кА/см²)
inserted in the microstrip line:
base electrode – NbTiN,
top - Al

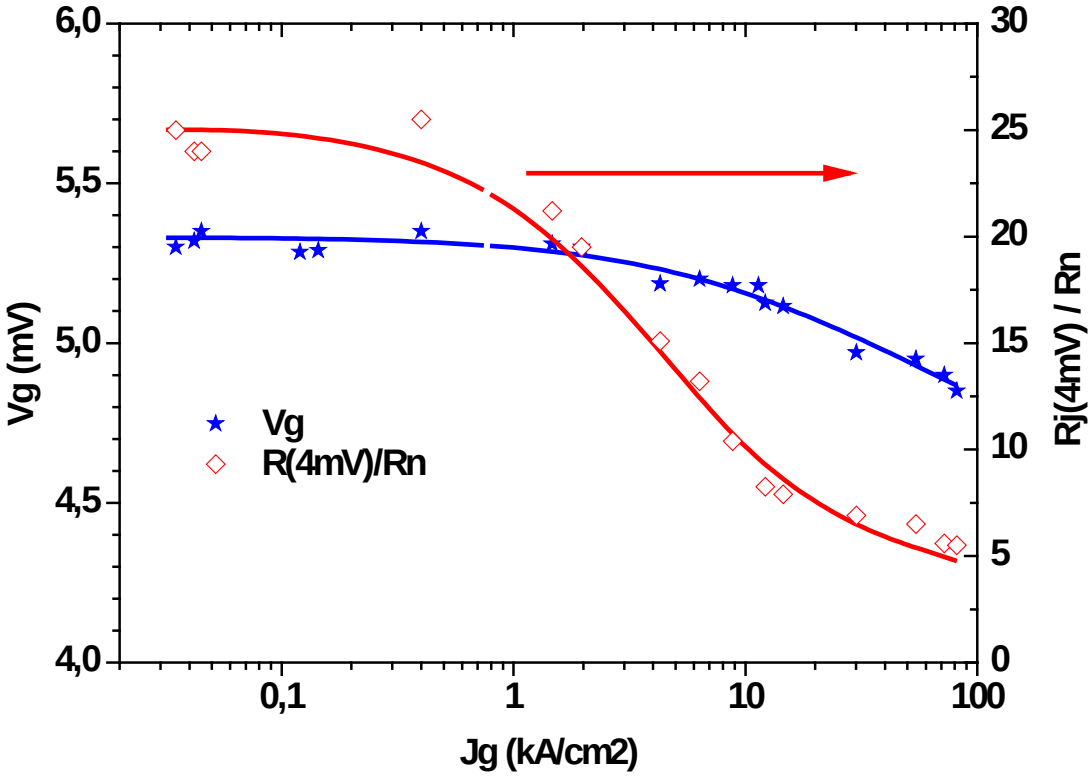




NbN-Mg/MgO-NbN SIS junctions

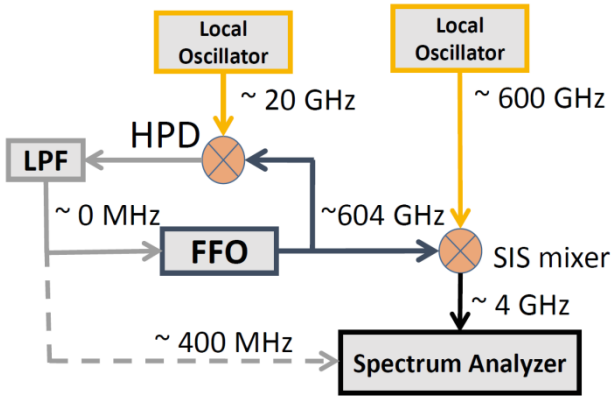


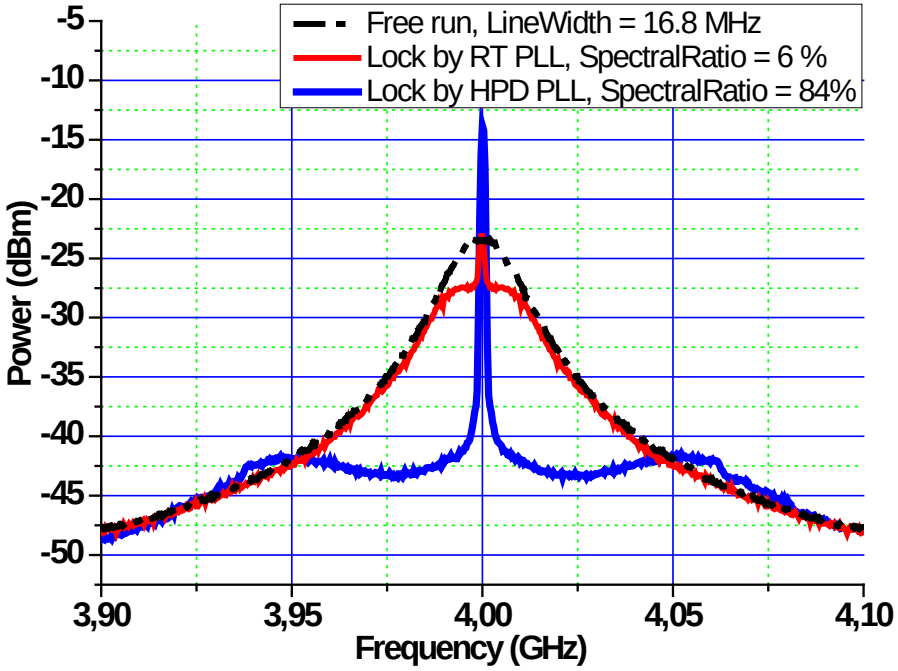




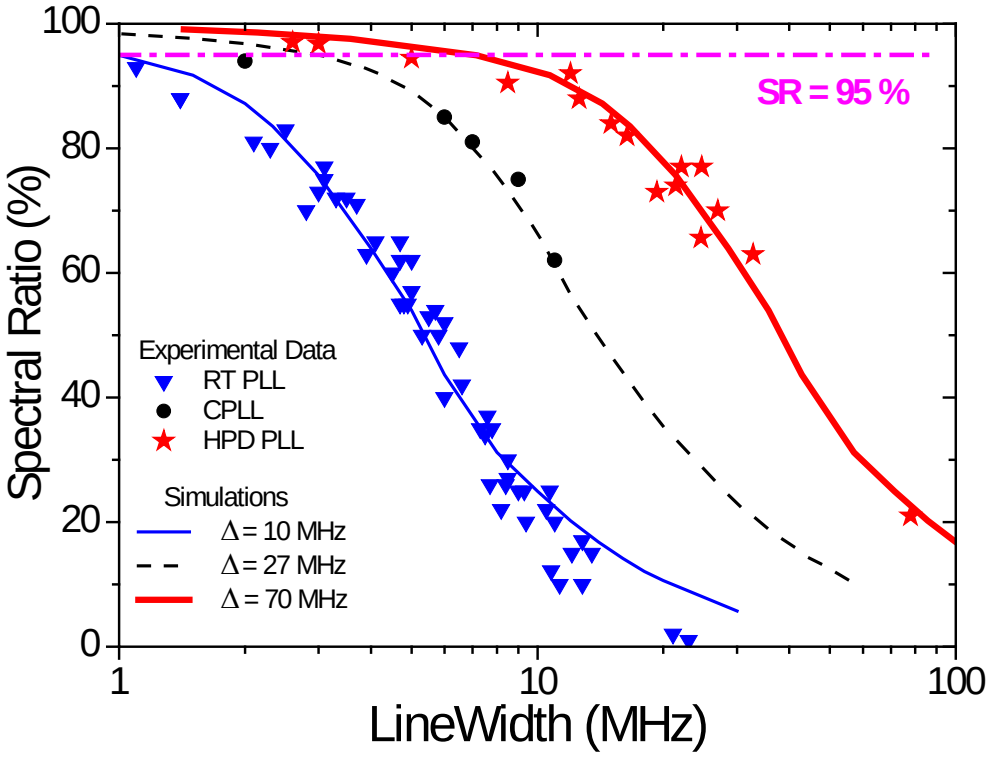
RnS = 80 Ω μm² ;
Jg = 6.3 kA/cm²
Vg = 5.06 mV;
Rn= 4.4 Ω;
Rj/Rn = 47;
R(4mV)/Rn = 15

Cryogenic Phase Detector
(new application of the SIS junction)



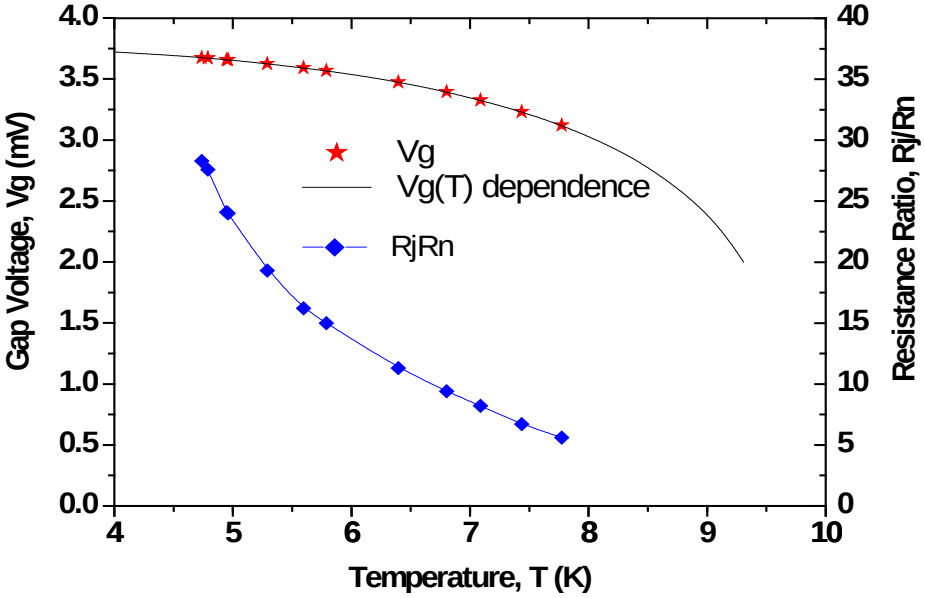


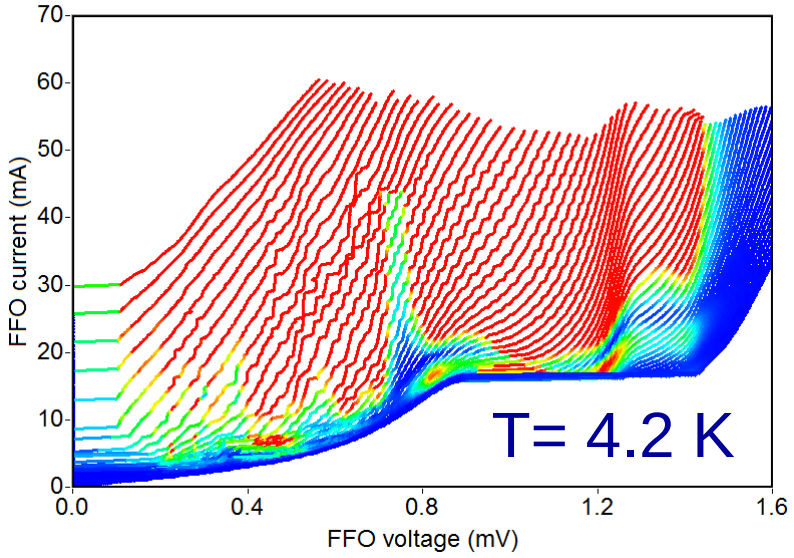
CHPD & FFO Integration

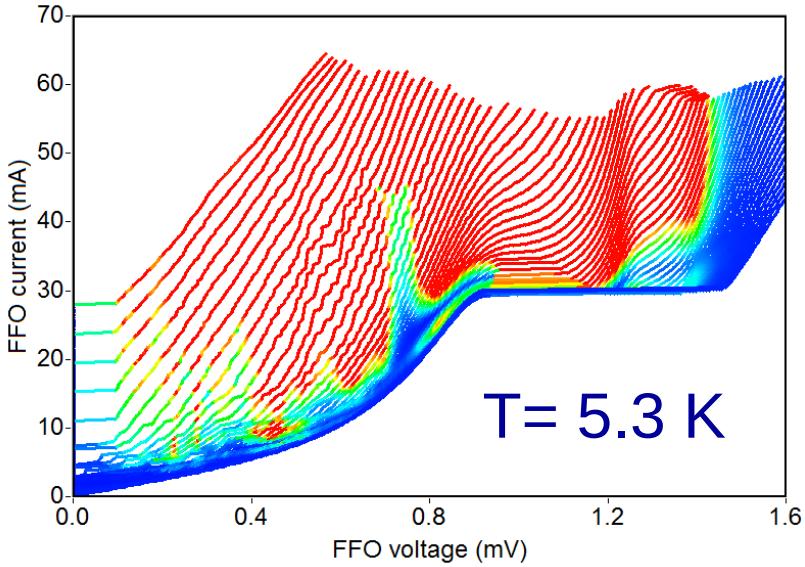


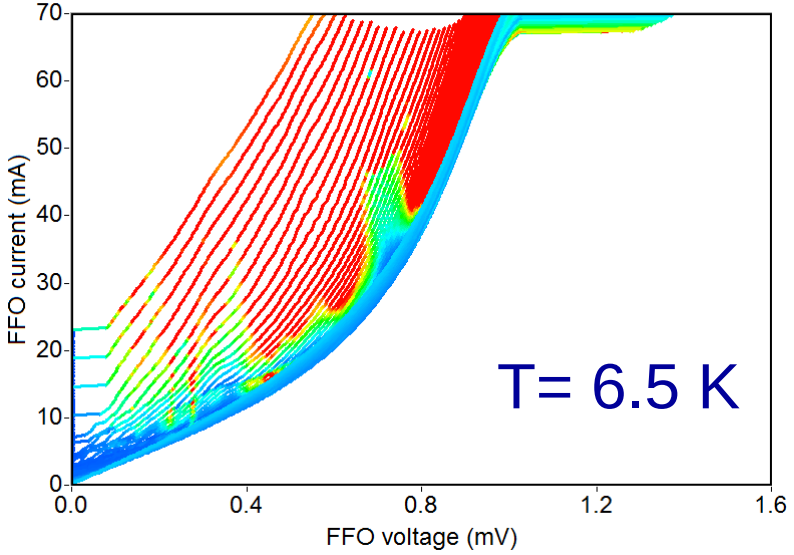
Bandwidth	Regular SM PLL	CryoPLL	CHPD
BW (МГц)	**12**	**40**	**70**

Thermal issue, challenge for the FFO / SIR









First RSFQ circuits

- K.K. Likharev, O.A. Mukhanov, and V.K. Semenov, “Resistive single flux quantum logic for the Josephson-junction digital technology,” in Proc. SQUID’85 (1985).
- V.P. Koshelets, K.K. Likharev, V.V. Migulin, et al., «Experimental Realization of a Resistive Single Flux Quantum Logic Circuit», IEEE Trans on Magn., V. MAG-23, No.2, p. 755, (1987).

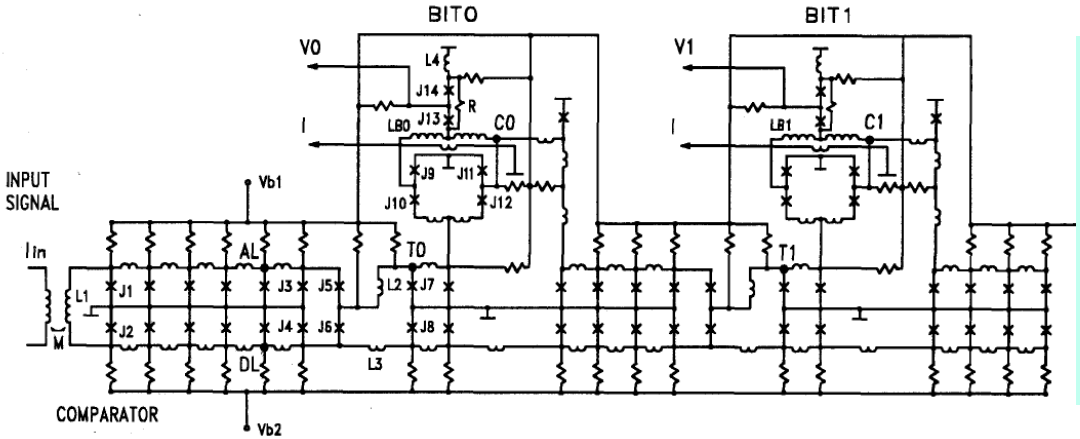


Fig.5 An equivalent circuit of A/D converter.

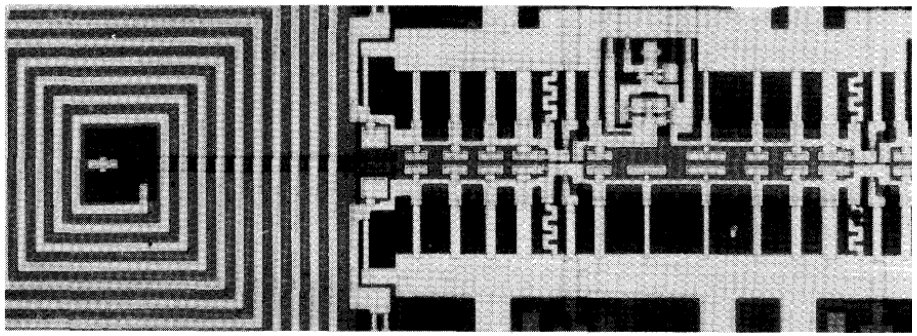


Fig.6 Microphotograph of A/D converter.

V.K. Kaplunenko, et al., «Experimental Implementation of SFQ NDRO Sells and 8-bit ADC», IEEE Trans on Applied Superconductivity, V. 3, No 1, pp 2662 - 2665, (1993).

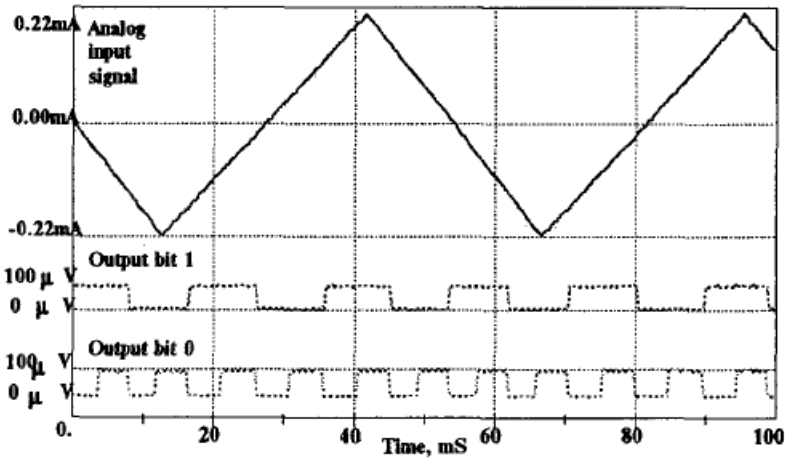


Fig.8 First two Bits A/D conversion output of rectangular input signal form.

Single Flux Quantum (SFQ) Autocorrelators

IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, VOL. 8, NO. 1, MARCH 1998

All-Digital 1-Bit RSFQ Autocorrelator for Radioastronomy Applications: Design and Experimental Results

Alexander V. Rylyakov and Stanislav V. Polonsky

1998

IEEE TRANSACTIONS ON APPLIED SUPERCONDUCTIVITY, VOL. 9, No. 2, JUNE 1999 3623

A Fully Integrated 16-channel RSFQ Autocorrelator Operating at 11 GHz.

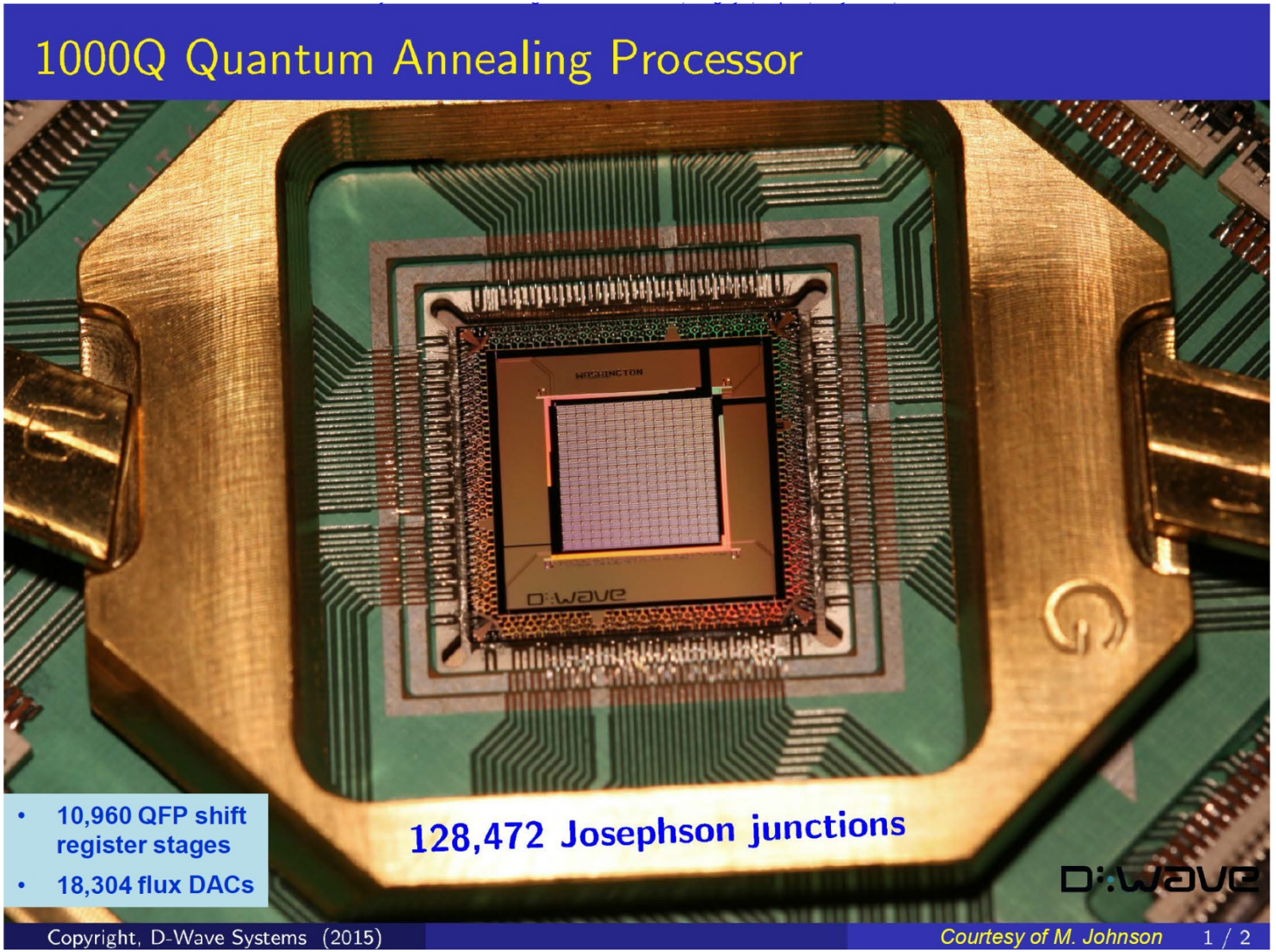
1999

A.V Rylyakov, D.F. Schneider and Yu.A. Polyakov
Department of Physics and Astronomy, State University of New York, Stony Brook, NY 11794–3800, USA

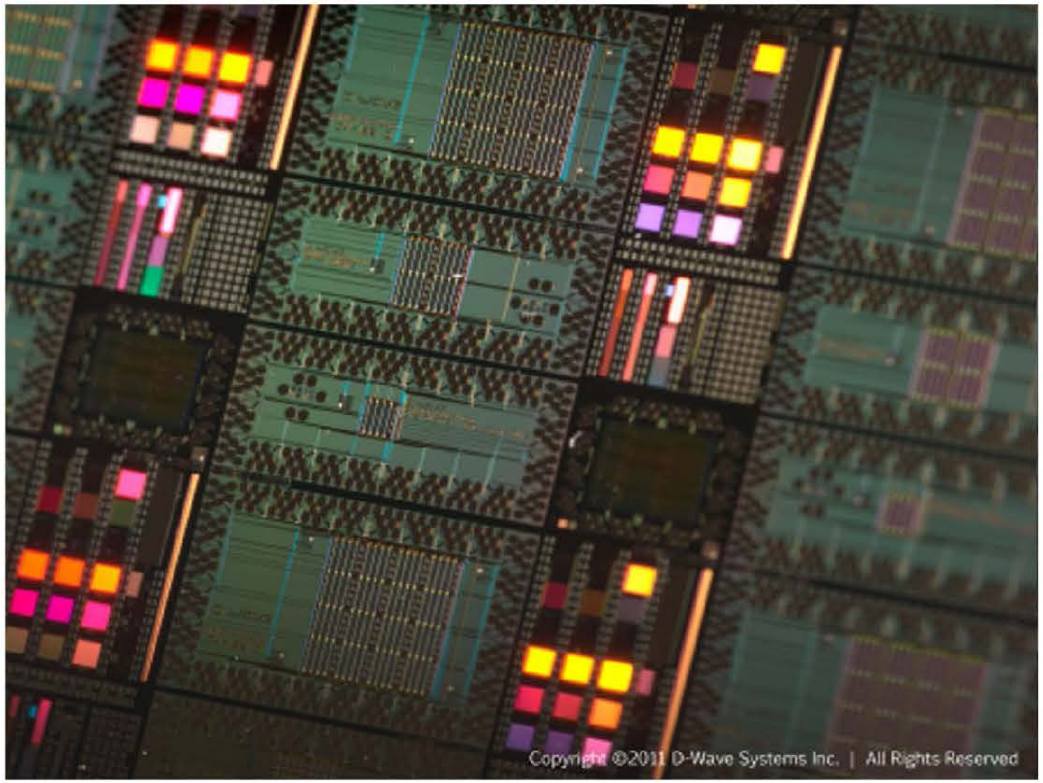
The 16-channel device, complete with a 16x9 array of binary counters, on-chip double-oversampling quantizer and on-chip clock was operational at clock speeds of up to **11 GHz**. The total number of Josephson junctions in the design was 1672, while the estimated total power dissipation was less than 0.1 mW (**6 μW per channel**). All chips were fabricated in HYPRES' standard 3.5-μm 10 μA/μm^2 Nb trilayer process.

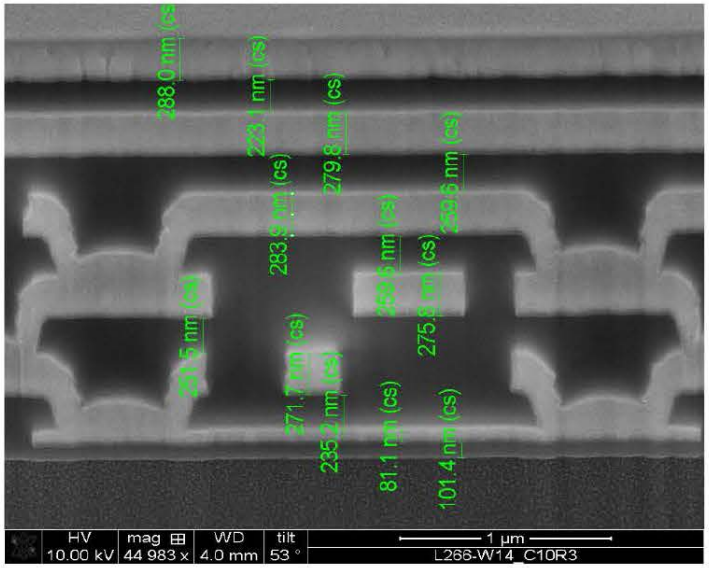
We also present a new concept of a 128-channel autocorrelator system built on 8 independent identical chips with approximately 2,500 Josephson junctions per chip. The projected parameters of the autocorrelator in 0.8 μm technology would feature clock speeds **above 100 GHz**, over 1,000 channels per single 5 x 5 mm^2 chip, **-100 dB** signal-to-noise resolution and power dissipation of **l μW** per channel.

SDE Fabrication: State of the Art (D-Wave)

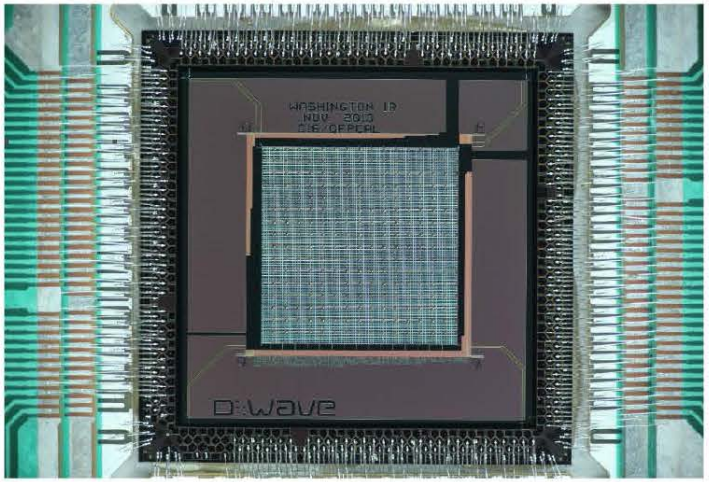


Superconductor fabrication at Cypress Semiconductor





- Nb/Al/AlOx/Nb trilayer process
- Six Nb wiring layers
- CMP SiO_2 dielectric
- 0.25μm lines & spaces

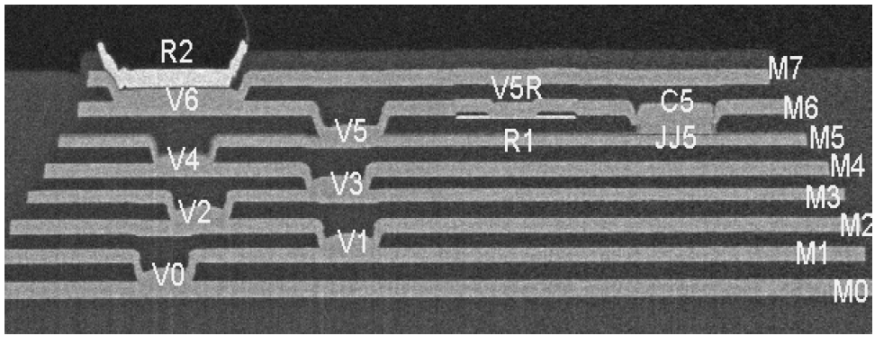


Courtesy of M. Johnson

MIT-LL Fully-Planarized SFQ Process

IARPA C3 Program

SFQ4ee 8-Nb-layer Process



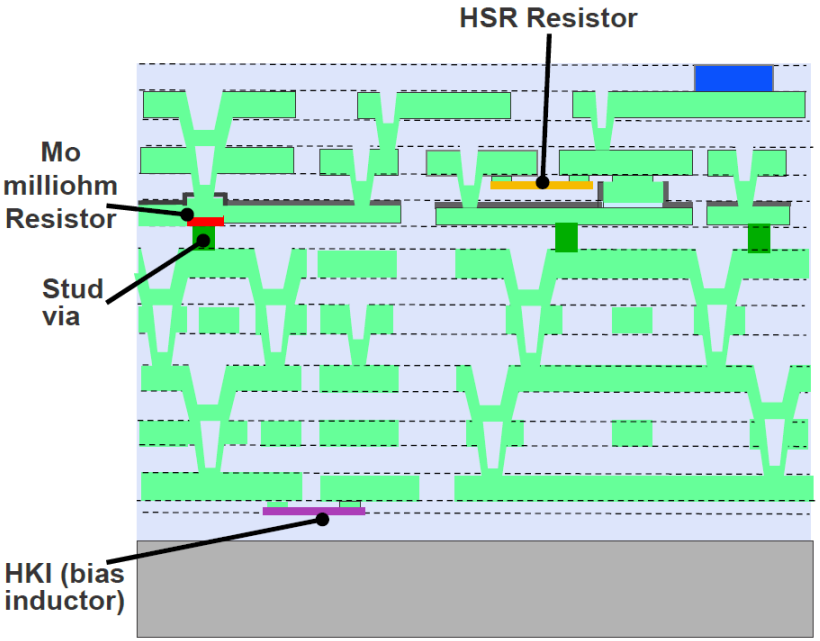
2 μm

SFQ4ee Process Features

- Primary 2015 process node
- 10 kA/cm^2 (100 μA/μm^2)
- Wafer size: 200-mm
- Min wiring feature size: 500 nm
- Min JJ size: 700 nm

To date, test circuits with 72K+ JJs per chip have been successfully demonstrated in the SFQ4ee process node.

SFQ5ee 8-Nb-layer Process (Fall 2015)

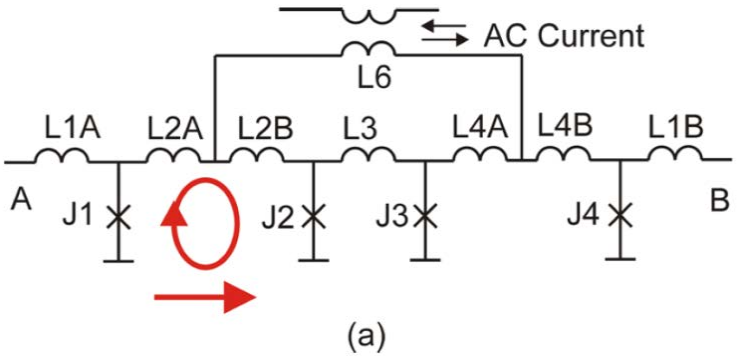


- High Kinetic Inductance (HKI) layer: 8 pH/sq
- High Sheet Resistance (HSR) option: 6 Ω/sq
- mΩ resistor
- Min wiring feature size: 350 nm
- Min JJ size: 700 nm

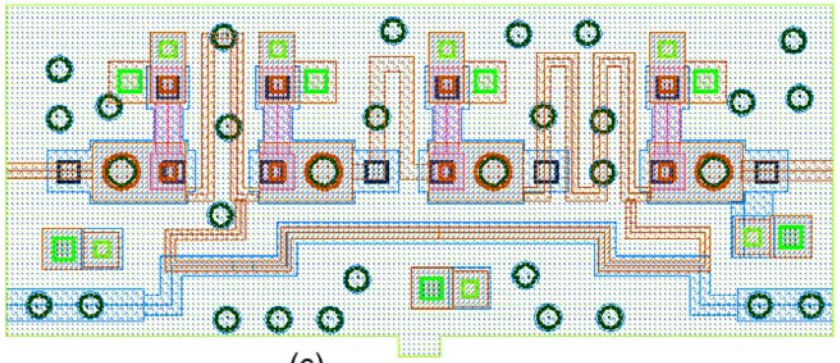
AC-Biased Shift Registers as Fabrication Process Benchmark Circuits and Flux Trapping Diagnostic Tool

Vasili K. Semenov, Yuri A. Polyakov, and Sergey K. Tolpygo

presented at the Applied Superconductivity Conference, Colorado, September 2016



(a)



(c)

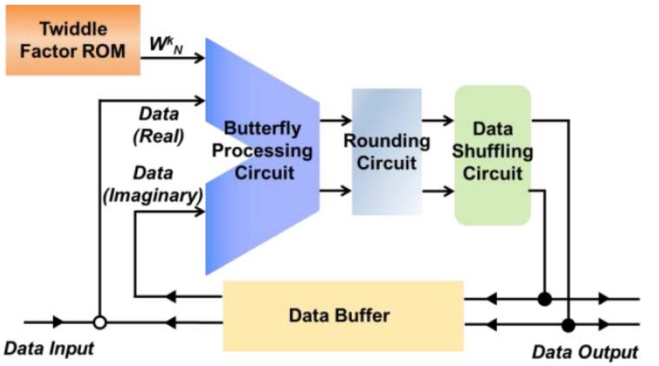
The shift registers having 202 thousand cells and, respectively, about 809 thousand Josephson junctions have been successfully tested. The circuits were fabricated at MIT Lincoln Laboratory, using a fully planarized process, 0.4 μm inductor linewidth and $1.33 \cdot 10^6/cm^{-2}$ junction density.

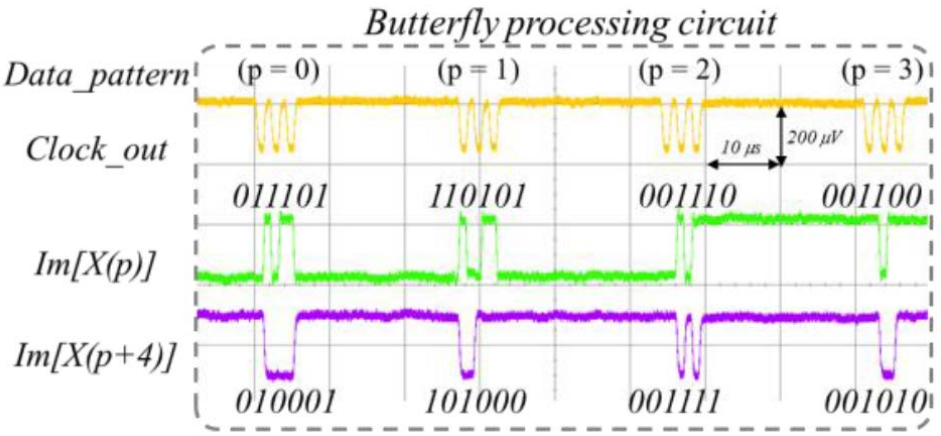
This is presently the largest operational superconducting SFQ circuits ever made. The-state-of-the-art in superconductor digital technology is close to the psychologically important million-junction level of integration. We have shown in this work that circuits with such level of integration can be designed, fabricated, and successfully tested.

Design and implementation of an SFQ-based single-chip FFT processor

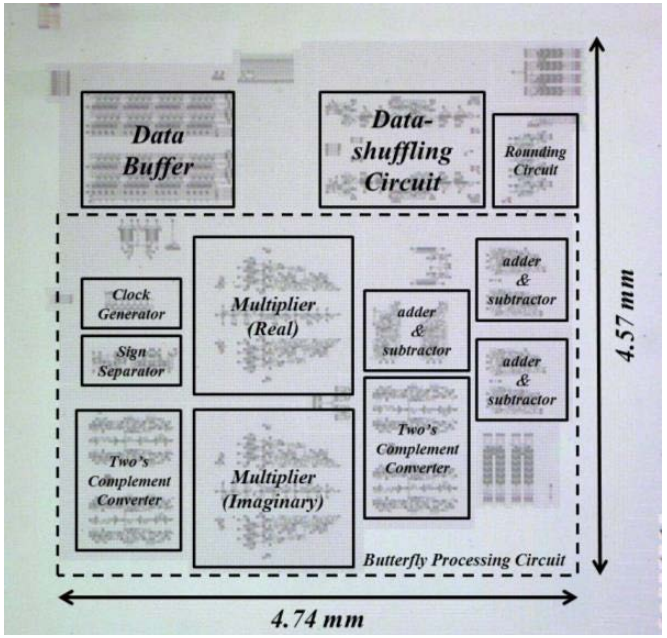
T. Ono, H. Suzuki, Y. Yamanashi, and N. Yoshikawa, Yokohama University, Japan;
Will be published in IEEE Transactions on Applied Superconductivity (2017)

All main elements of the high-speed FFT processor based on single-flux-quantum (SFQ) logic circuits have been designed and fabricated using the AIST 10 kA/cm^2 Nb advanced process 2 (ADP2). These elements were successfully tested at a target frequency of 50 GHz. SFQ-based single-chip FFT processor integrating all the component circuits has been designed; full function for the first stage single-chip FFT processor was confirmed.





Output data patterns for imaginary part at high speed



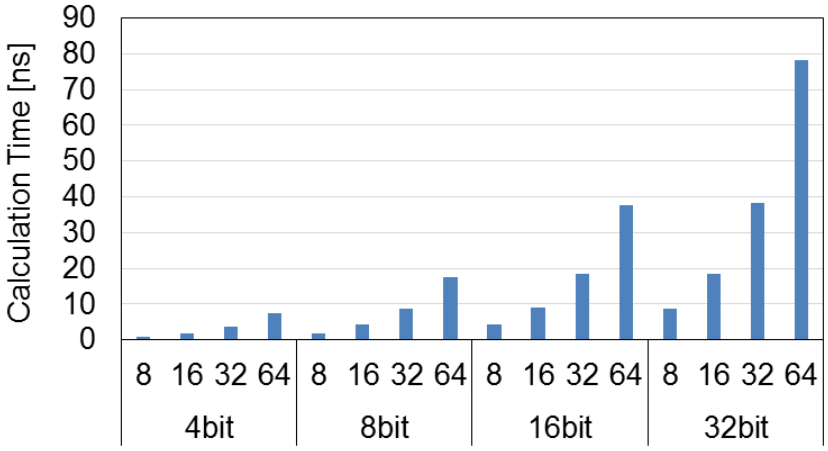
Estimations for SFQ-based single-chip FFT processors

The SFQ-based FFT processor for the 12-bit 64-point FFT is expected to have a calculation time of 27.8 ns with 50 GHz local clock frequency and power consumption of 36 mW. With the introduction of the LR-biased SFQ circuit, the power consumption could be reduced by a factor of 10 to realize 3.6 mW.

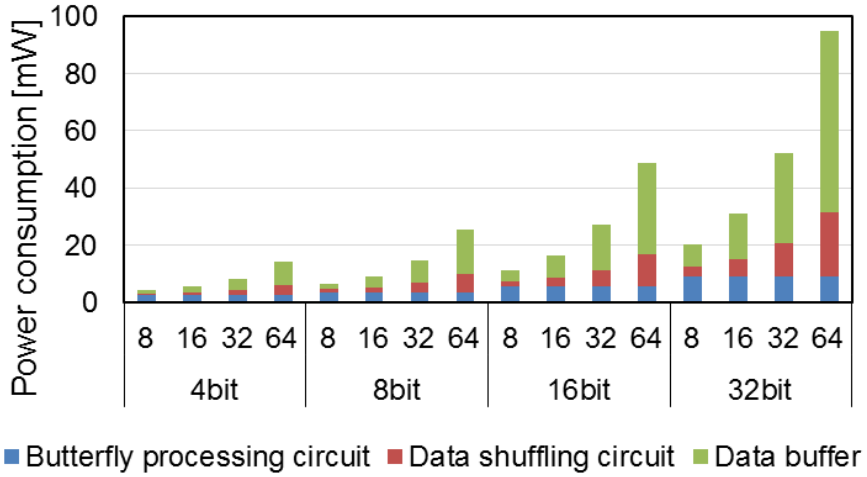
	Technology	FFT points	Bit-width	Power [mW] [3]	Processing time [ns]
CMOS FFT [1]	0.18 μm	64	12	21.43	640
SFQ FFT [2]	ADP2	64	12	3.6	27.8

[1] T.H. Tran, *et al*. Low-Power and High-Speed Chips (COOL CHIPS XIX), 2016 IEEE Symposium, 2016.
[2] Y. Sakashita, et al, *15th International Superconductive Electronics Conference, ISEC* 2015
[3] Introducing low-power techniques such as LR-biasing.

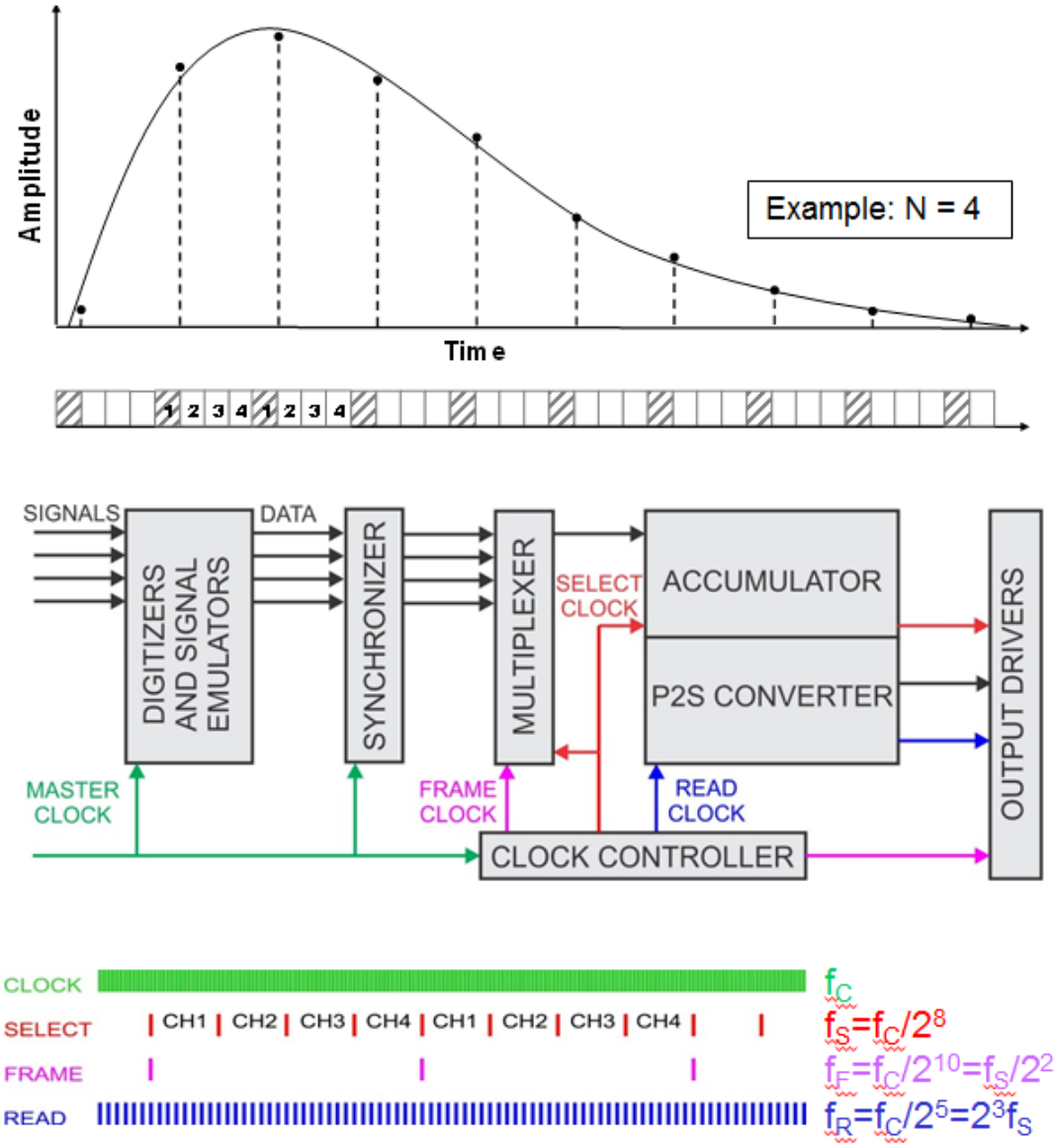
Calculation time vs. circuit scale



Power consumption vs. circuit scale



Digital Time Division Multiplexing Readout Circuit

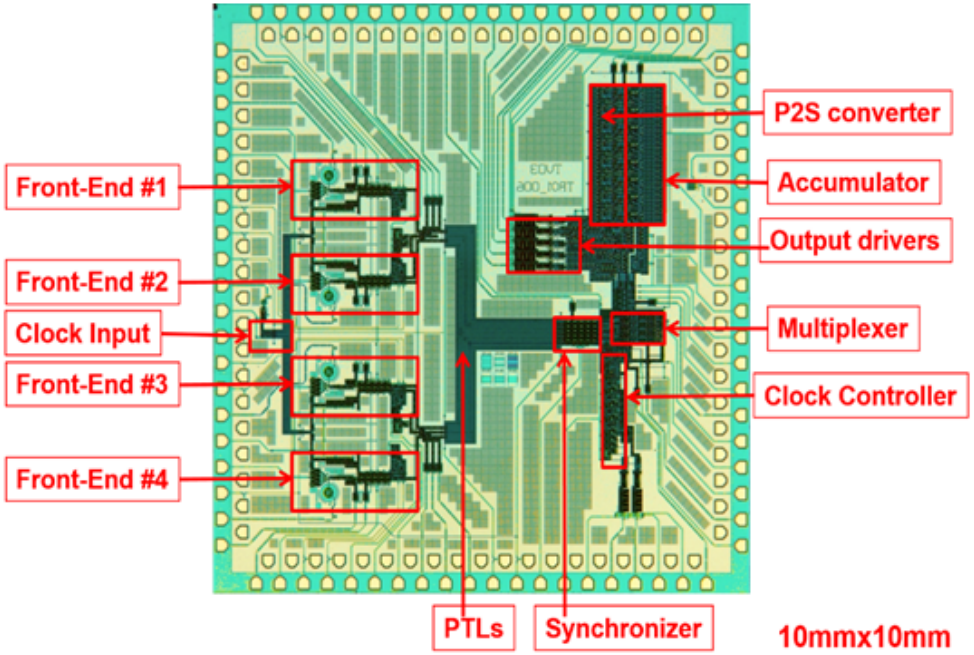


- **Outputs from N sensors are digitized, multiplexed and processed in a common digital back-end**
  - Digitizers are SQUIDs, either synchronous or asynchronous
  - Digital multiplexer consists of an array of switches
  - Back-end is a digital counter (accumulator) followed by parallel-to-serial (P2S) converter
- **Design uses RSFQ and ERSFQ circuitry on the same chip**
  - ADC: RSFQ
  - Multiplexer: ERSFQ
  - Digital Back-end: ERSFQ
  - Output Drivers: RSFQ

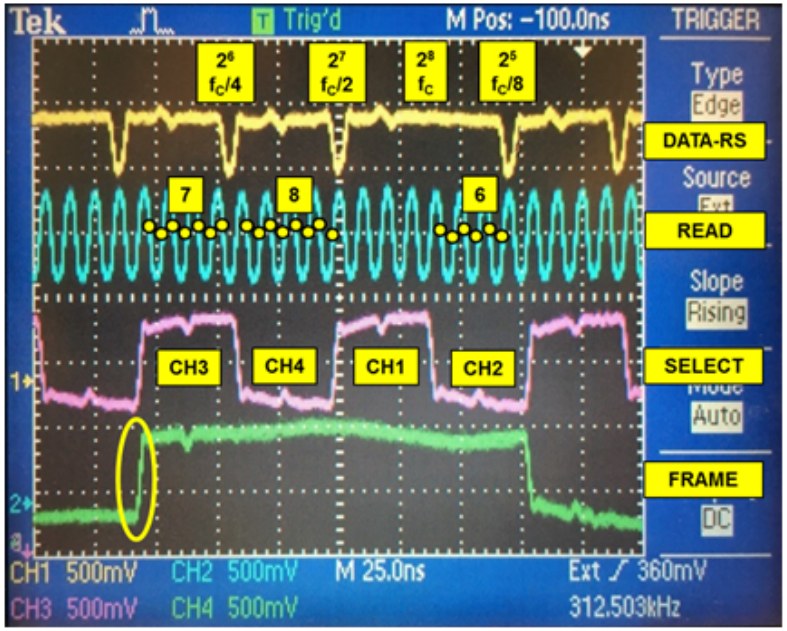
Courtesy of T. Filippov

Digital Time Division Multiplexer Chip

Digital TDM Readout Chip (10mm × 10mm)



High-Frequency Testing @ 12.8 GHz

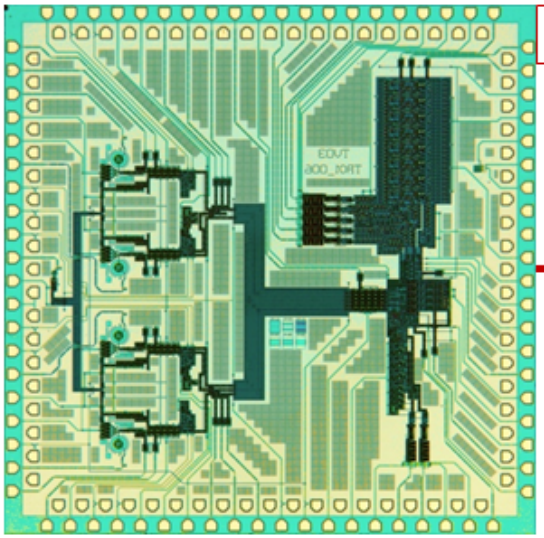


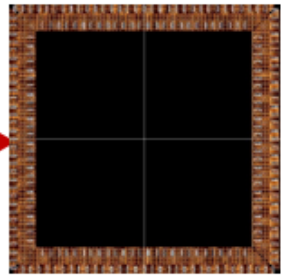
- 4 input channels (4 ADCs and embedded pattern generators for testing)
- Correct operation at frequencies up to 12.8 GHz
- Chip fabricated with HYPRES 4-layer 4.5 kA/cm^2 process

Courtesy of T. Filippov

A. Sahu, T. Filippov, M. Radparvar, D. Kirichenko, D. Gupta, "Digital Time-Division Multiplexing Readout Circuit for Sensor Arrays," IEEE Transactions on Applied Superconductivity 27 (4), 1-6, 2017

Design Exercise: 100-channel TDM Readout





$$N = T_{pulse}/(2^m k T_{clk})$$

Example:
k = 8 samples/pulse
m = 8 bits/sample
T_{pulse} = 10 μs
T_{clk} = 50 ps
N ~ 100

- **Area:**
  - **Usable Chip Area ≥ 16 mm² on a 5mm x 5mm chip**
  - **Area of shared digital back-end: < 1 mm² (MITLL 10 kA/cm²)**
    - **8 mm² (on demonstrated HYPRES 4.5 kA/cm² chip), cell library scaling factor: 9**
  - **Area of sensitive DC SQUID: 0.06 mm²**
  - **Area of contact pad: 0.08 mm²**
  - ✓ **100 channels can fit on a 5mm x 5mm chip**
- **Power:**
  - **Shared ERSFQ Digital Counter and Serializer**
  - ✓ **200-500 μW for 100 channels**

Courtesy of T. Filippov

Conclusion

- Concept of the Superconducting Integrated Receiver (SIR) with phase-locked FFO is developed and proven. The SIR technology is mature enough for laboratory applications as well as for ground-based and even space radio astronomy; nevertheless the SIR is not “off-the-shelf product” yet.
- There is some room for further FFO/SIR improvement, although trade off between performance and operational parameters should be considered. A well-defined program with long-term financial support is required to start further development.
- A number of superconducting Single Flux Quantum (SFQ) circuits and devices are under development for data digitizing and processing. Ultimate parameters of the SFQ devices surpass considerably the figures for existing CMOS circuits, although the SFQ digital technology is still remaining on the “demonstrator” level.

Thank you for your attention